AN ABSTRACT OF THE THESIS OF

Dingming Xie for the degree of Master of Science in Electrical and Computer Engineering presented on October 14, 1999.

Title: LOW FREQUENCY NOISE AND THE UPCONVERTED PHASE NOISE EFFECTS IN NMOSFET CIRCUITS

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Abstract approved:

Leonard Forbes

The literature on flicker noise in n-MOSFET's is reviewed. The two main sources of low frequency flicker noise are mobility fluctuations and number fluctuations due to surface states. Our experiments on NMOS noise measurements were done for both the subthreshold and the saturation regions of operation for both long channel (5 μm) and short channel (as small as 0.6 μm) NMOS transistors. The results suggest that for both types that in the saturation region, the flicker noise is due to the surface state effect and the noise equations, NLEV = 2 and 3, in SPICE, HSPICE and PSPICE are most appropriate. For short channel devices, due to the effects of velocity saturation and the resulting non-linear transconductance (gm) variation with gate bias voltage, the input-referred voltage noise increases as the gate-source voltage increases instead of staying constant as it does for long channel devices. In the subthreshold region, the input-referred voltage noise decreases drastically as the gate-source voltage increases for both long channel and short channel NMOS devices. Simulations have been done using

PSPICE and HSPICE, with noise level (NLEV) = 3 and device model level 3 and BSIM3.2 & 3.3. The results from PSPICE level 7 (BSIM3.3) and SPICE level 3 compare favorably with the measured noise phenomena for the short channel and long channel NMOS devices respectively.

The other part of this work describes a successful simulation using HSPICE and comparison to published data of the phase noise on a 2-GHz CMOS LC oscillator caused by low frequency flicker noise ($1/f$ noise). The flicker noise, which is determined by experimental measurements on NMOSFETs transistors, is simulated as a sum of sine waves with random phase by using MATLAB, and is finally introduced into the LC oscillator circuit as a HSPICE piecewise linear waveform. The output of LC oscillator in HSPICE is written as a series of points equally spaced in time and then the spectrum is computed by fast Fourier transform (FFT). The simulation results show the phase noise of the VCO with different KF values, and demonstrate the phase noise caused by low frequency flicker noise has a $1/f^3$ dependence on the offset frequency. The difference between the simulated sideband power spectral density and the measured values reported in the literature is small.

Index Terms—$1/f$ noise, phase noise, MOSFET, n-channel, subthreshold, saturation, input-referred noise, drain current noise, SPICE model, measurement, simulation, LC oscillator, fast Fourier transform (FFT), MATLAB, KF value, $1/f^3$, offset frequency.

LOW FREQUENCY NOISE AND THE UPCONVERTED PHASE NOISE EFFECTS IN NMOSFET CIRCUITS

by

Dingming Xie

A THESIS

submitted to

Oregon State University

in partial fulfillment of

the requirement for the degree of

Master of Science

Presented October 14, 1999

Commencement June, 2000

Master of Science thesis of Dingming Xie presented on October 14, 1999

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ACKNOWLEDGEMENT

I would like to express my sincere and deep appreciation to my major professor and academic advisor, Dr. Leonard Forbes, for his warm encouragement and competent guidance and untiring help throughout the study. Without his help, this thesis would never have been possible.

Special thanks are extended to my minor professor, Dr. S. Subramanian for his wonderful teaching on semiconductor processing courses and good advices.

I also would like to express my deep appreciation to Dr. Gabor Temes and Dr. Un-Ku Moon for their excellent teaching on analog circuits and wonderful advices for my thesis research.

Thanks to my group members, Kam-Fai So, Fenard Thenus and Mark Cheng for their helpful comments and cooperation.

Special thanks to Lei Wu for his academic discussion and personal help.

Thanks to the National Science Foundation Center for the Design of Analog/Digital Integrated Circuits (CDADIC) for the generous financial supports.

This thesis is dedicated to my parents, Youman Xie and Muxiang Luo, my sisters, my brothers, my dearest friend Qun Jing and her parents for their constant encouragement and support.

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I. INTRODUCTION

There are two groups of noise sources, device noise and interference. Device noise includes thermal, shot and flicker noise, while interference includes substrate and power supply noise. All these noise sources can up-convert into close-in phase noise by being introduced into oscillator circuits.

Flicker noise is also known as $1/f$ noise, because the noise spectral density is inversely proportional to frequency. It is a major noise source in silicon MOSFET's, especially in the low frequency range. It places a lower limit on the level of signal detection and spectral purity, so it is important for a circuit designer to minimize this effect in order to improve circuit performance. As low power and low voltage electronic devices are becoming more and more popular, the effect of low frequency flicker noise becomes more and more important and it is more difficult to provide enough dynamic range and better circuit performance.

A large number of studies of flicker noise in MOSFET's have been made over the period 1957 to 1998 [1]-[41], but there still is no generally accepted model for both p- and n-channel MOS transistors.

Basically, all the discussions can be divided into two kinds of thoughts on the origin of $1/f$ noise, carrier density fluctuation (due to surface states) model, also called

McWhorter ΔN model, and mobility fluctuation (due to bulk effect) model, also called Hooge Δμ model.

According to the first ΔN model, the flicker noise is caused by tunneling of free-charge carriers into oxide traps close to the Si-SiO_2 interface, the input referred voltage noise will be independent of the gate bias voltage and the magnitude of the noise spectra is proportional to the interface trap density. Experimental data reveal that the slope η of the $1/f^{\eta}$ noise spectra varies from 0.7 to 1.2, instead of the exact 1.

According to the second Δμ model, the stochastic nature of carrier scattering events cause the low frequency noise, and it suggests a gate bias voltage dependence on the input-referred voltage noise.

Inconsistent experiment results have been published for both NMOS and PMOS. Also, different models are introduced in different versions of SPICE (SPICE, HSPICE and PSPICE) for $1/f$ noise of MOSFET's. For example, the HSPICE manual provides three different models for the drain current flicker noise and are designated by different model levels (0-3):

For NLEV = 0 $$I_{flick}^2 = KF \cdot I_{drain}^{AF} / (C_{OX} \cdot L_{eff}^2 \cdot f) \quad (1)$$

For NLEV = 1 $$I_{flick}^2 = KF \cdot I_{drain}^{AF} / (C_{OX} \cdot W \cdot L_{eff} \cdot f) \quad (2)$$

For NLEV = 2 & 3 $$I_{flick}^2 = KF \cdot gm^2 / (C_{OX} \cdot W \cdot L_{eff} \cdot f^{AF}) \quad (3)$$

There are two parameters KF and AF where a range of values for KF is suggested as being from 10^{-19} to 10^{-25} V^2 F. The units here are even not consistent with some of the equations. There is also no suggestion as to which equation is more appropriate for NMOS and PMOS, and under what kind of condition it is appropriate to use, long channel or short channel devices, saturation region or subthreshold region.

Voltage-controlled oscillators (VCO) are an integral part of phase-locked loops (PLL) used in clock recovery circuits and frequency synthesizers. Besides resonant RLC oscillators used in RF circuits, inductorless ring oscillators have demonstrated potential in high speed phase locked systems. In both cases actual oscillators exhibit skirts around the center frequency due to the modulation of the oscillation by not only white noise but also $1/f$ noise. The demand for more available channels in the wireless communication applications, such as mobile cell phones, has imposed more stringent requirements on the phase noise of local oscillators (LO). Phase noise, in the guise of jitter in the digital world, limits the immunity of the receiver's LO against nearby interference signals. And phase noise in the transmitter LO can overwhelm nearby weak channels. Therefore it is very important to research the phase noise effects on oscillators.

The study of phase noise in CMOS oscillators has been investigated both theoretically and experimentally [42]-[46]. Razavi [42] also showed some SPICE simulation of oscillators by injecting a white noise and/or sinusoidal current noise. Unfortunately, he found that in his simulation, the magnitude of the sidebands did not directly scale with the magnitude of the injected noise.

A general theory of phase noise in electrical oscillators has been proposed by A. Hajimiri and T. H. Lee [43]. It predicts the existence of $1/f^3$, $1/f^2$, and flat regions for the phase spectrum quantitatively by the following expressions:

$$P_{SBC}\{\Delta\omega\} = 10 \cdot \log \{I_n \cdot C_n / (4 \cdot q_{max} \cdot \Delta\omega)\}^2 \tag{4}$$

$$L\{\Delta\omega\} = 10 \cdot \log \{[\Gamma_{rms}^2 / q_{max}^2] \cdot [(i_n^2/\Delta f) / (4 \cdot \omega^2)]\} \tag{5}$$

$$L\{\Delta\omega\} = 10 \cdot \log \{[C_0^2 / q_{max}^2] \cdot [(i_n^2/\Delta f) / (8 \cdot \Delta\omega^2)] \cdot [\omega_{1/f}/\Delta\omega]\} \tag{6}$$

Where (4) is the general equation for the sideband power relative to the carrier, (5) and (6) are the equations derived from (4) for the phase noise sideband power spectral density (PSD) in the $1/f^2$ and $1/f^3$ regions respectively. It shows that the $1/f^3$ portion is due to the low frequency flicker noise, while the $1/f^2$ portion is due to the white noise.

In this paper, the research was divided into two parts to be illustrated. In the first part, Section II, we try to ascertain which model is most appropriate for NMOS transistors (both long channel and short channel) under both subthreshold and saturation operating conditions. The sub-Section II.A explains how we experimentally measure the flicker noise and process the data by using fast Fourier transform (FFT). The sub-Section II.B shows how we try to match the experimental results for the flicker noise by doing SPICE simulation, including both HSPICE and PSPICE, by using different device models and noise models. The sub-Section II.C gives the results and discussions.

In the second part of the research, Section III, we do the phase noise research in a 2-GHz CMOS LC oscillator. First, we apply a time variant noise, which simulates the flicker noise, to a cross-coupled CMOS LC voltage controlled oscillator. The sub-Section III.A explains the procedure to simulate the random-phase flicker noise by using MATLAB based on the experimental results and HSPICE noise models. The sub-Section III.B shows the HSPICE simulation of the phase noise effect on a LC oscillator by introducing flicker noise into the oscillator circuit. The simulation results of the phase noise sideband PSD in the LC oscillator is compared to published results. We conclude with a demonstration of how the simulation method can be used to quantify the phase noise in LC oscillators. The sub-Section III.C gives a summary of the simulation process and results.

II. LOW FREQUENCY FLICKER NOISE IN N-MOSFET'S

The work is initially addressed at large micron size NMOS devices (5-um channel length) experimentally and by simulation in saturation region, then moved on to the more difficult problems of sub-micron devices (0.6-um and 1.2-um channel length) and subthreshold models.

A. n-MOSFET NOISE MEASUREMENT

Two kinds of approaches are used to determine the n-MOSFET's low frequency noise. One is an automated measurement, which measures the amplified differential NMOS drain voltage variation over a time period, and then uses a fast Fourier transform (FFT) to process the experimental data and get the desired noise (drain current noise and input-referred voltage noise) in the frequency domain. Fig. 2.1 shows the schematic of the automated noise measurement system for NMOS transistors. The NMOS transistor is connected upside down with negative power supplies to its gate (Vgg) and source (Vss). This serves to reduce any power supply noise effect at the drain node. The voltage drop across the drain resistor, Rd, is measured by a voltmeter. Thus, the small-signal transconductance used in the calculation of input-referred noise can be calculated from measurements of drain current variations with gate-to-source voltage. The amplifiers are made from commercially available IC operational amplifiers. A first order filter is used to amplify the weak noise signal, which provides a gain of 45 with cutoff frequency of 21 kHz. A Tektronix DM 5010 Programmable Digital Multimeter (DMM) is used to sample

the experimental data in time domain. Because the sampling frequency of DMM is only 26 Hz, a fourth order Butterworth filter with gain of 2 is designed to lower the signal corner frequency from 21 kHz to 4.2 Hz. Thus the total system can measure the flicker noise at frequencies below 4.2 Hz and has a total gain of 90. The system background noise is measured by replacing the NMOS transistor with a resistor that has about same DC resistance as the transistor.

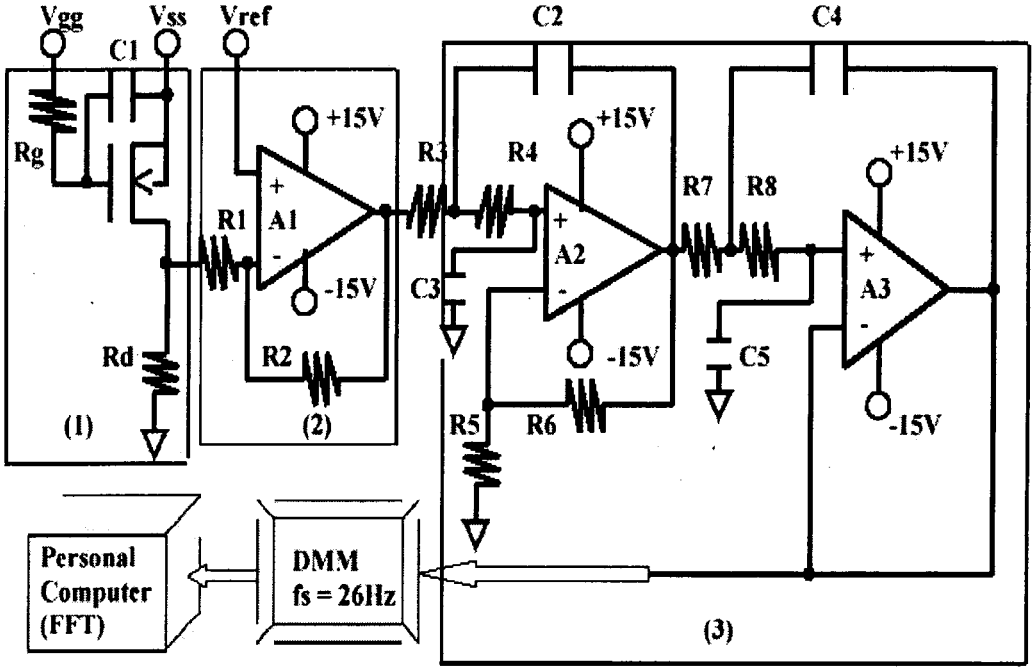

Figure 2.1. Schematic of automated NMOS noise measurement setup.
(1) NMOS transistor under test; (2) 1st order filter, Gain = 45, fc = 21 kHz;
(3) 4th order Butterworth filter, Gain = 2, fc = 4.2 Hz.

The other is an analog measurement, which using Princeton Applied Research Model 184 Current Sensitive Preamplifier as a frequency selective RMS voltmeter. The

transistor setup is same as the one used previously in the automated setup. The drain current noise can be directly measured at a particular frequency. The input-referred voltage noise can be obtained in the same way as in the automated method, by calculating the transconductance, gm, first. Due to power line frequency harmonics, the drain current noise at frequencies lower than 1 kHz can not be easily measured.

The NMOS transistors to be measured are: (i) long channel transistors with W = 120 μm, L = 5 μm, VTO = 1.4 V and TOX = 1050 Å; (ii) short channel transistors, including 1.2 μm ones with W = 30.8 μm, L = 1.2 μm, VTO = 0.7 V and TOX = 100 Å, and 0.6 μm ones with W = 30.8 μm, L = 0.6 μm, VTO = 0.7 V and TOX = 100 Å.

B. n-MOSFET NOISE SIMULATION

Device model levels, level 3, BSIM3.2 (i.e., level 6 in PSPICE and level 47 in HSPICE) and BSIM 3.3 (i.e., level 7 in PSPICE and level 49 in HSPICE) are tried for long channel and short channel devices respectively to fit their experimental DC characteristics, including the drain current, Ids, and the transconductance, gm. The parameters in the models, such as the oxide thickness, TOX, and the intrinsic transconductance parameter, KP, are adjusted for the best match. Once the appropriate model is found for each individual device, the noise characteristics can be simulated according to the noise experimental results using the appropriate noise equation selector (NLEV, or NOIMOD), flicker noise exponent (AF) and coefficient (KF) in SPICE (see Table 2.1 for details about the device models and noise models, also see the Appendix part of this thesis).

Table 2.1 NMOSFET noise simulation

Simulation Tools		HSPICE	PSPICE
Device model	SPICE level 3	Level 3 (noise model default: NLEV = 2)	Level 3 (noise model default: NLEV = 2)
	BSIM 3.2	Level 47 (noise model default: NLEV = 2)	Level 6 (noise model default: NLEV = 2)
	BSIM 3.3	Level 49 (noise model default: NLEV = 2)	Level 7 (noise model default: noimod= 1)
Noise model	Noise model in SPICE level 3	NLEV = 0: $\overline{I_{nd}^2} = \frac{KF \bullet I_{ds}^{AF}}{C_{OX} \bullet L_{eff}^2 \bullet f}$ NLEV = 1: $\overline{I_{nd}^2} = \frac{KF \bullet I_{ds}^{AF}}{C_{OX} \bullet W_{eff} \bullet L_{eff} \bullet f}$ NLEV = 2 & 3 (default): $\overline{I_{nd}^2} = \frac{KF \bullet g_m^2}{C_{OX} \bullet W_{eff} \bullet L_{eff} \bullet f^{AF}}$	Same as left
	BSIM 3.2	Same as above	Same as above
	Noise model in BSIM 3.3	Same as above	noimod = 1 (default): $\overline{I_{nd}^2} = \frac{KF \bullet I_{ds}^{AF}}{C_{OX} \bullet L_{eff}^2 \bullet f^{ef}}$ (1) noimod = 2 (2):

Note: (1): According to our data, we believe that this expression should be NLEV=2 &3;

(2): The noimod = 2 noise model is as following from BSIM3.3 manual:

$$\overline{I_{nd}^2} = \frac{q^2 kT\mu_{eff} I_{ds}}{C_{OX} L_{eff}^2 f^{ef} \bullet 10^8}\{Noia \bullet \log\{\frac{N_0 + 2\times 10^{14}}{N_l + 2\times 10^{14}}\} + Noib \bullet (N_0 - N_l)$$

$$+ \frac{Noic}{2}\{N_0^2 - N_l^2)\} + \frac{V_{tm} I_{ds} \Delta L_{clm}}{W_{eff} L_{eff}^2 f^{ef} \bullet 10^8} \bullet \frac{Noia + Noib \bullet N_l + Noic \bullet N_l^2}{(N_l + 2\times 10^{14})^2}$$

C. RESULTS AND DISCUSSIONS

Both long channel (L = 5.0 μm) and short channel devices (L = 1.2 μm and 0.6 μm) have been measured in both the saturation and the subthreshold regions of operation.

An example of the Digital Multimeter output in time domain is shown as Fig. 2.2, the measurement is done with 5-μm NMOS transistors with Vss = -12 V and Vgs = 4 V in the saturation region (Vgs > Vt).

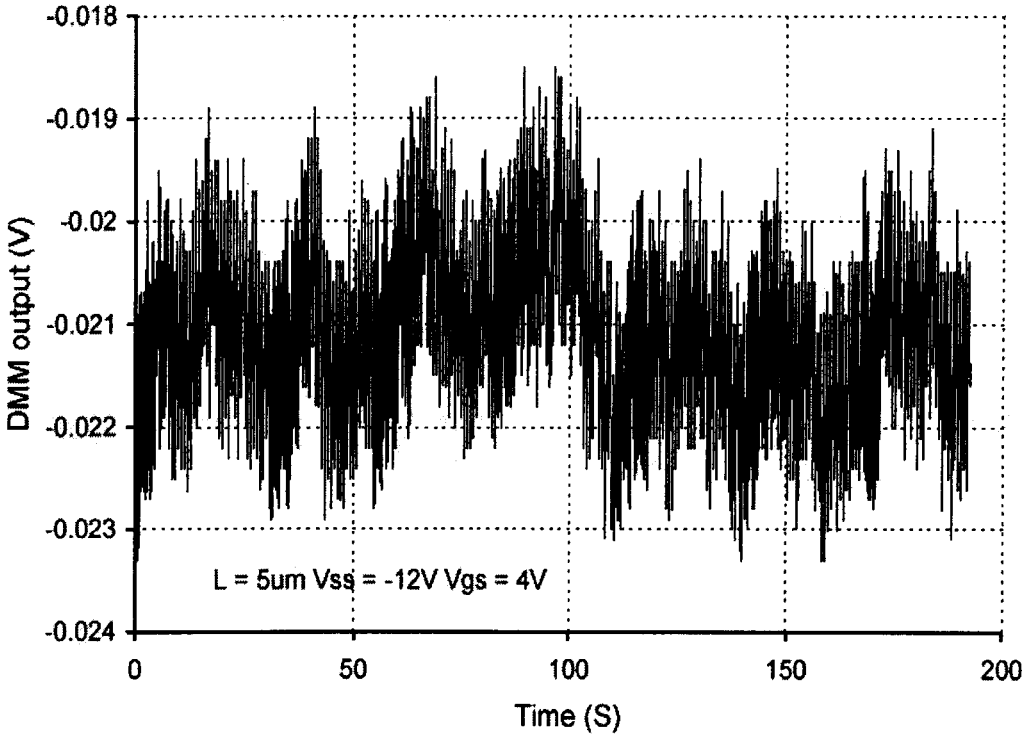

Figure 2.2. Digital Multimeter output voltage in time domain.
NMOS: W = 120 um, L = 5.0 μm, Vss = -12 V, Vgs = 4 V.

Fig. 2.3 shows the corresponding power spectral density (PSD) of the measured 5-μm NMOS input-referred voltage noise after a FFT. The flicker noise exponent, AF, is close to 1.0. This figure also shows the noise measured by analog techniques at 1 kHz for the 5-μm device at the same condition, and the 1-kHz-noise for 1.2-μm and 0.6-μm NMOS devices under the saturation condition with Vss = -5 V, Vgs = 2.5 V. The extrapolation at 1-kHz of the automated measured $1/f$ noise fits well with the measured noise at 1-kHz by analog techniques for the 5-μm NMOS transistor.

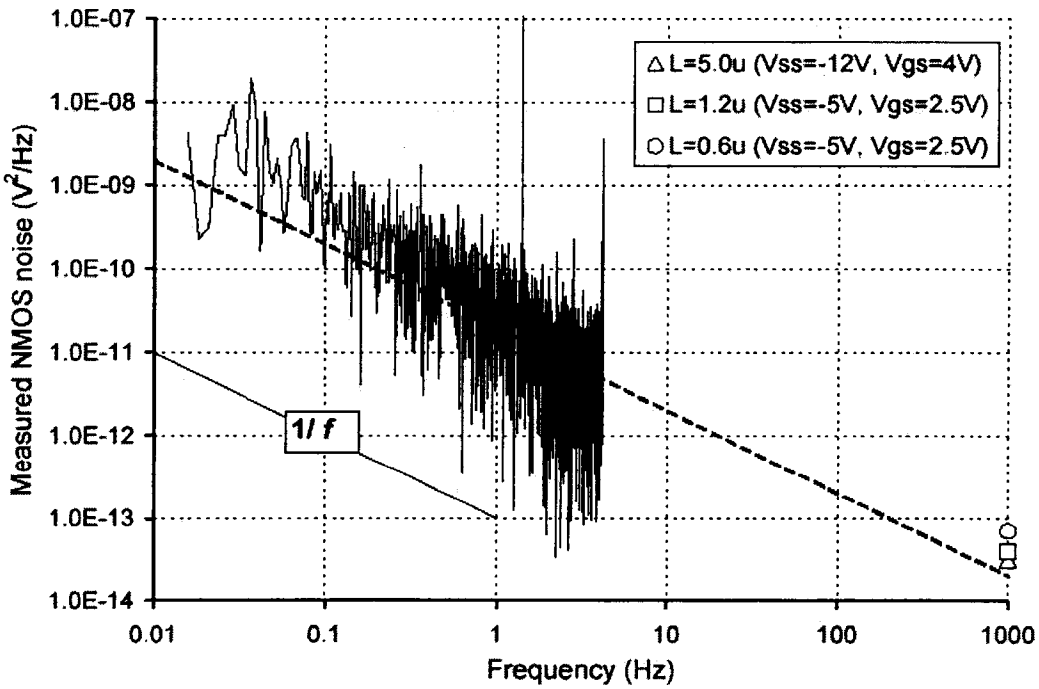

Figure 2.3. Power spectral density (PSD) of measured NMOS input-referred noise.
(i) 5-μm devices: Vss = -12 V and Vgs = 4 V.
(ii) 0.6-μm devices: Vss = -5 V and Vgs = 2.5 V.
(iii) 1.2-μm devices: Vss = -5 V and Vgs = 2.5 V.

The SPICE simulations show that the device model level 3 is the most appropriate for the long channel 5-um transistors (see Fig. 2.4), while level 7 in PSPICE, i.e., BSIM 3.3 is the most appropriate to model the DC characteristics of the short channel devices (shown in Fig. 2.5 for 0.6-um NMOS only). The parameters used are: TOX = 1050 Å and KP = 22 $\mu A/V^2$ for 5-μm NMOS devices; and TOX = 95 Å and KP = 50 $\mu A/V^2$ for both 1.2-μm and 0.6-μm NMOS devices. As we will see later, the measured input-referred noise results shows that the noise model, NLEV = 3 with AF = 1 in SPICE simulation is most appropriate.

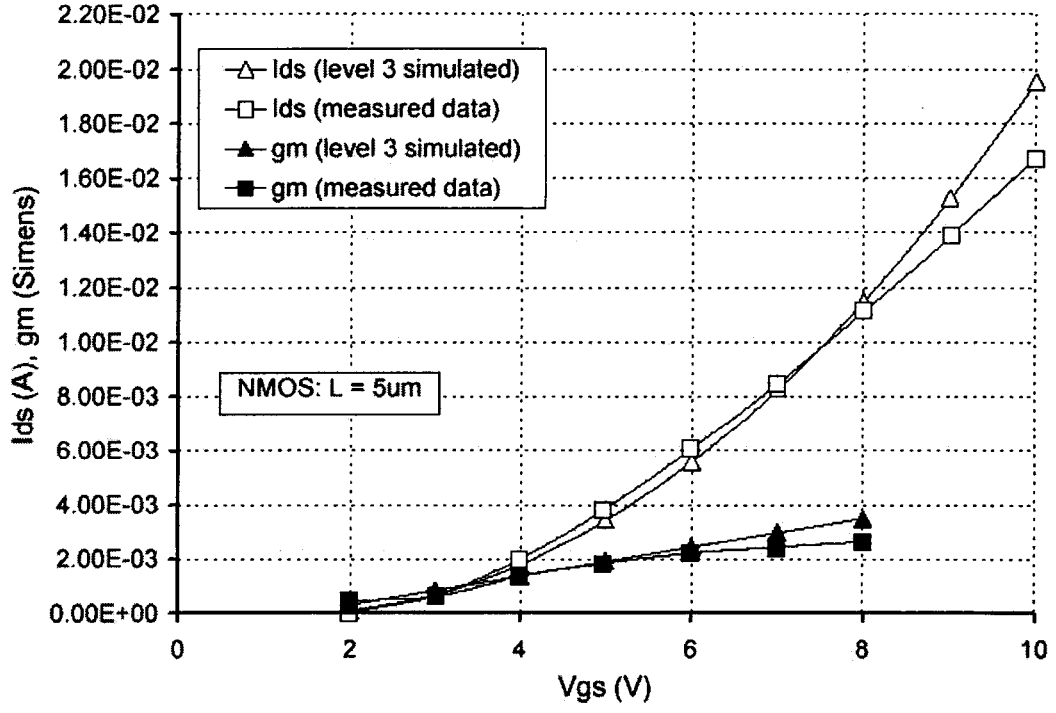

Figure 2.4. Measured and simulated DC characteristics of the 5-um NMOS transistors. SPICE level 3 to simulate when TOX = 1050 Å and KP = 22 $\mu A/V^2$.

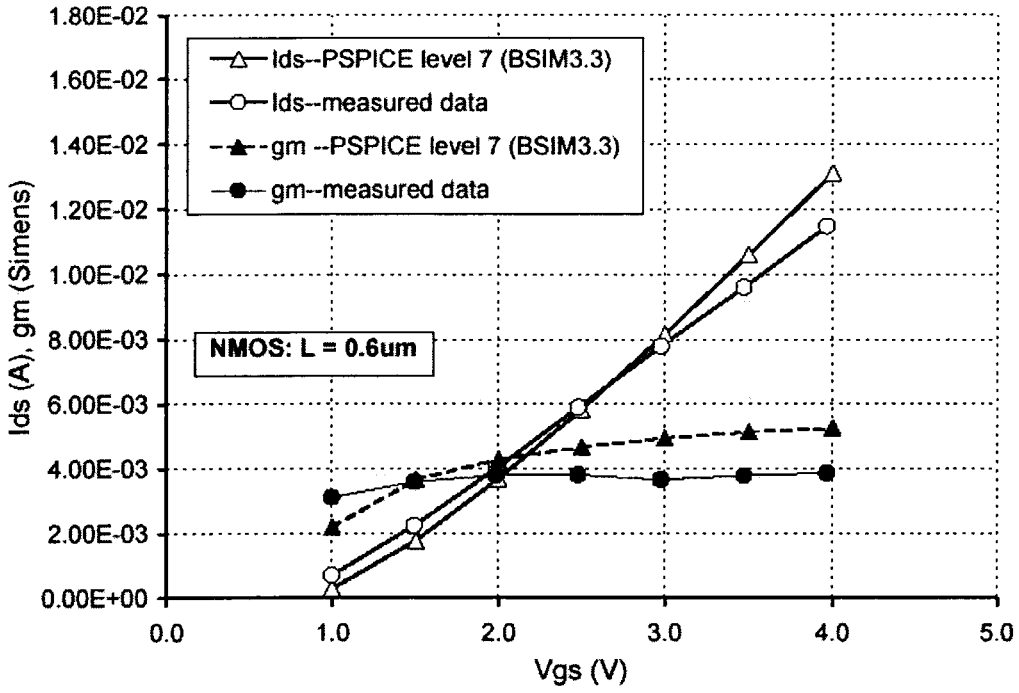

Figure 2.5. Measured and simulated DC characteristics of the 0.6-um NMOS transistors. PSPICE level 7 (BSIM 3.3) to simulate when TOX = 95 Å and KP = 50 $\mu A/V^2$.

Thus, the measured noise results have been compared to the surface state model for noise in SPICE, NLEV = 3 with AF =1, using the device model level 3 for the long channel, 5-μm devices, and the BSIM3.3 (level 7 in PSPICE) for the short channel, 1.2-μm and 0.6-μm devices. The KF value is 1.05e-23 V^2 F for the 5-μm NMOS devices, and 1.0e-24 V^2 F for the 1.2-μm and 0.6-μm NMOS devices.

Fig. 2.6 shows the simulated and measured NMOS mean square drain current noise versus absolute gate-source voltage in the saturation region for L = 5.0 μm, 1.2 μm and 0.6 μm respectively at frequency of 1.0 Hz. It shows that the shorter the NMOS transistor channel, the larger the mean square drain current noise. The slopes of all these

three treadlines are close to 2, which demonstrate that the mean square drain current noise (Ind^2) is proportional to the square of the absolute gate voltage (Vgs), that is,

$$\overline{I_{nd}{}^2} \propto Vgs^2$$

But from the measured data in this figure, we can not conclude which model is the most appropriate because all the equations, Eqn. 1, Eqn. 2 and Eqn. 3, show this relationship if we set AF equals to 1, due to the relationships of drain current, Ids, proportional to Vgs^2 and transconductance, gm, proportional to Vgs.

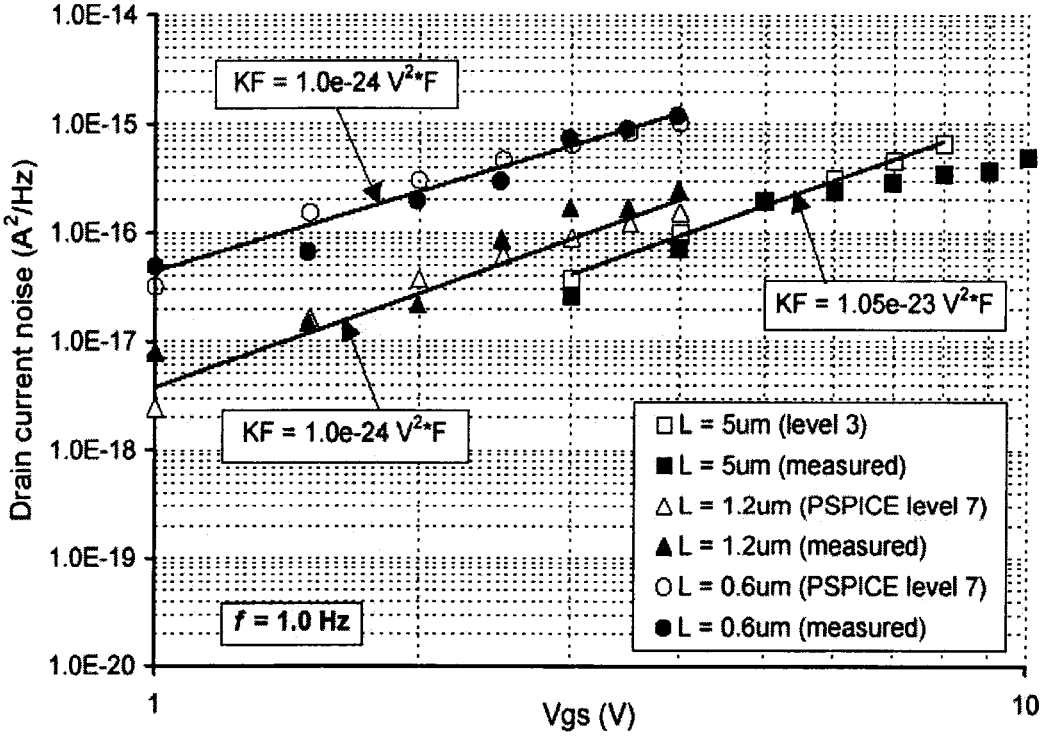

Figure 2.6. Simulated and measured NMOS drain current noise versus absolute gate-source voltage in the saturation region. L = 5.0 μm, 1.2 μm and 0.6 μm respectively. f = 1 Hz.

Fig. 2.7 shows the corresponding simulated and measured NMOS input-referred voltage noise in the saturation region.

For the simple case of 5-um-long channel devices, from the measured data in Fig. 2.7, we can see that the surface states model, Eqn. 3 (NLEV = 2 or 3) is the most appropriate since the input referred voltage noise is independent of the gate bias voltage. That may be because that for the long channel NMOS devices, the transconductance, gm, is a linear function of gate voltage, Vgs, in the saturation region, and so the input referred noise stays constant.

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \mu C_{OX} \frac{W}{L}(V_{gs} - V_T)$$

So, from Eqn. 3, we can have

$$\overline{V_{ng}^{\,2}} = \frac{\overline{I_{nd}^{\,2}}}{g_m^{\,2}} = \frac{KF}{C_{OX} W L_{eff} f}$$

For the 0.6-um and 1.2um-short channel devices, however, from the measured data in Fig. 2.7, we can not see clearly whether the surface states model still applies because the input referred voltage noise increases when increasing the gate bias voltage. But the simulation using PSPICE level 7 tells us that the surface states model does still apply. In fact, the simulation results in both Fig. 2.6 and Fig. 2.7, from level 3 and PSPICE level 7 for the long channel and short channel devices respectively, match very well to the experimentally measured data. This suggest that for both long channel and short channel NMOS devices, the flicker noise is originated from the carrier density fluctuation, i.e., the surface states ΔN model.

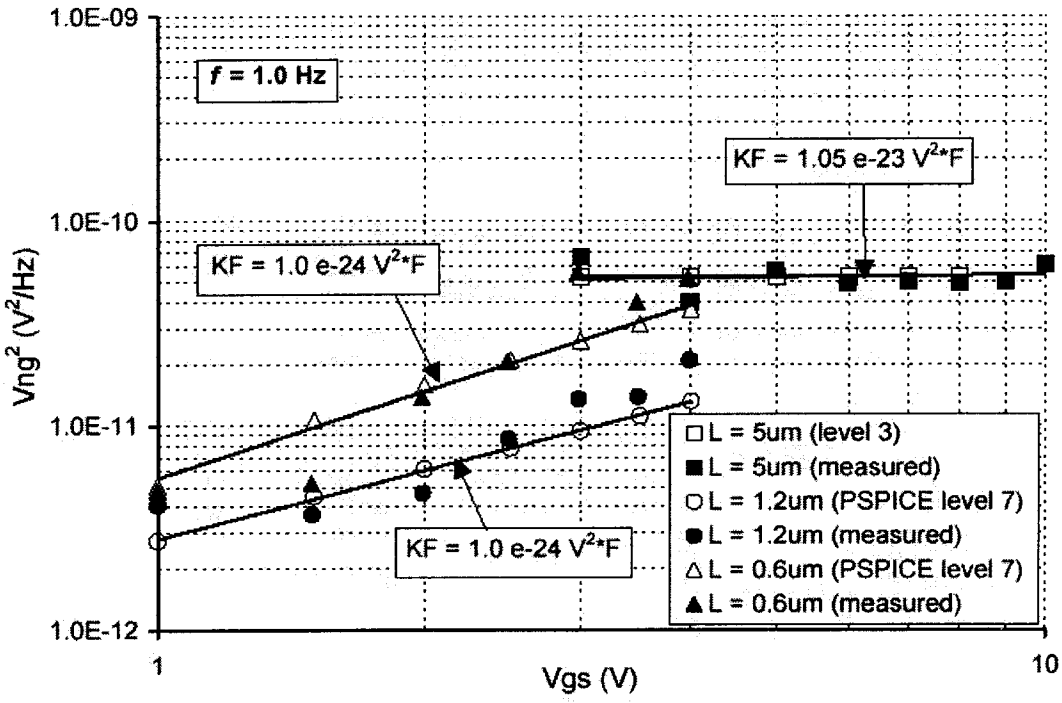

Figure 2.7. Simulated and measured NMOS input-referred voltage noise versus absolute gate-source voltage in the saturation region.
L = 5.0 μm, 1.2 μm and 0.6 μm respectively. $f = 1$ Hz.

The reason for that in the short channel NMOS devices, the input referred voltage noise shows the dependence on the gate bias voltage may be because that, due to the velocity saturation of carriers in the channel, the transconductance does not increase linearly with gate voltage bias [17].

Considering the presence of velocity saturation effects, the drain current of MOSFET working in situation region is:

$$I_{DS} = \frac{\mu C_{OX}}{2\left[1+\theta(V_{GS}-V_t)\right]}\frac{W}{L}(V_{GS}-V_t)^2$$

where $\theta = 1/L\xi_C$, (ξ_C, electric field) and has the dimension V^{-1}. It can be shown that the transconductance under short channel effects is:

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{\mu C_{OX}}{2}\frac{W}{L}\frac{2(V_{GS} - V_t) + \theta(V_{GS} - V_t)^2}{[1 + \theta(V_{GS} - V_t)]^2}$$

So, the transconductance, gm, is no longer linear with the gate voltage, Vgs.

Fig. 8 shows the transconductance characteristics obtained by analytical calculation from the above equation, by PSPICE level 7 simulation and experimental measurement for 0.6um-NMOS devices over a range of gate bias.

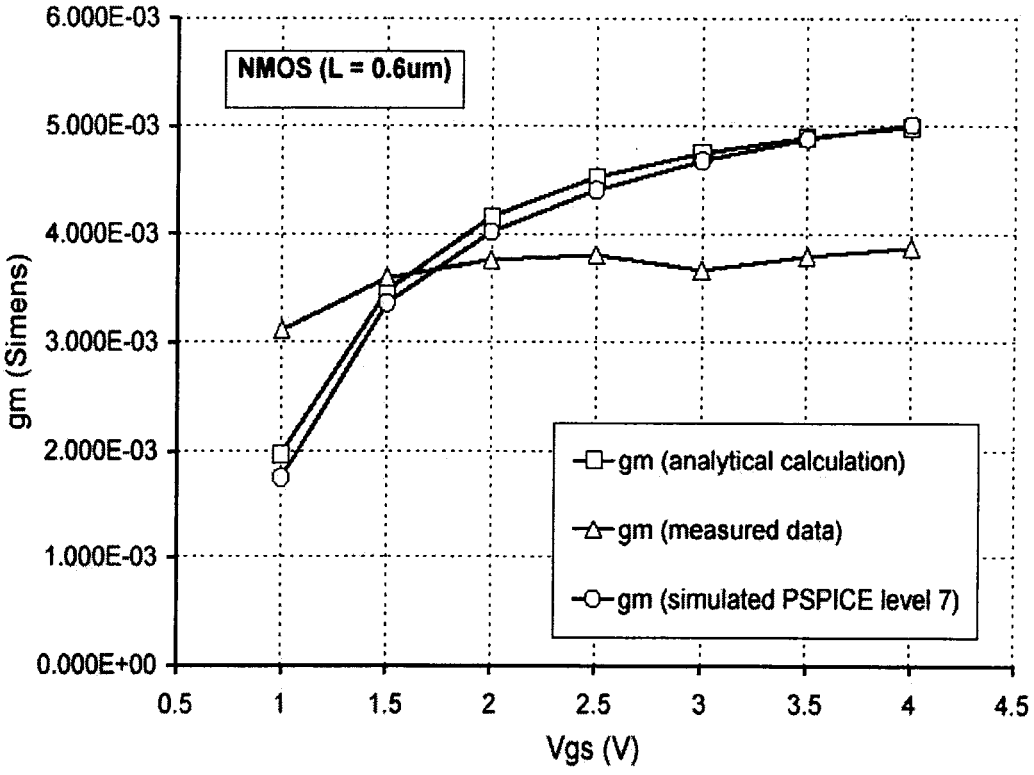

Figure 2.8. Short channel effects on 0.6um-NMOSFET transconductance.

This Fig. 2.8 demonstrates that the transconductances increase more slowly with increasing gate bias. This non-linearity of the transconductance causes the input referred voltage noise at the gate to increase with increasing gate bias in the saturation region. There appears to be an error in the HSPICE BSIM 3.3 (level 49) noise model, for input referred noise voltage. It appears to be calculated using a transconductance which changes linearly with gate voltage even for submicron devices.

Fig. 2.9 and Fig. 2.10 show that the HSPICE BSIM 3.2 (level 47) and PSPICE BSIM 3.2 (level 6) give almost the same results as that of the HSPICE BSIM 3.3 (level 49). Although they can approximately simulate the drain current noises close to the measured ones as shown in Fig. 2.9, they can not show that the input referred gate voltage noise increases proportionally when increasing gate bias as shown in Fig. 2.10.

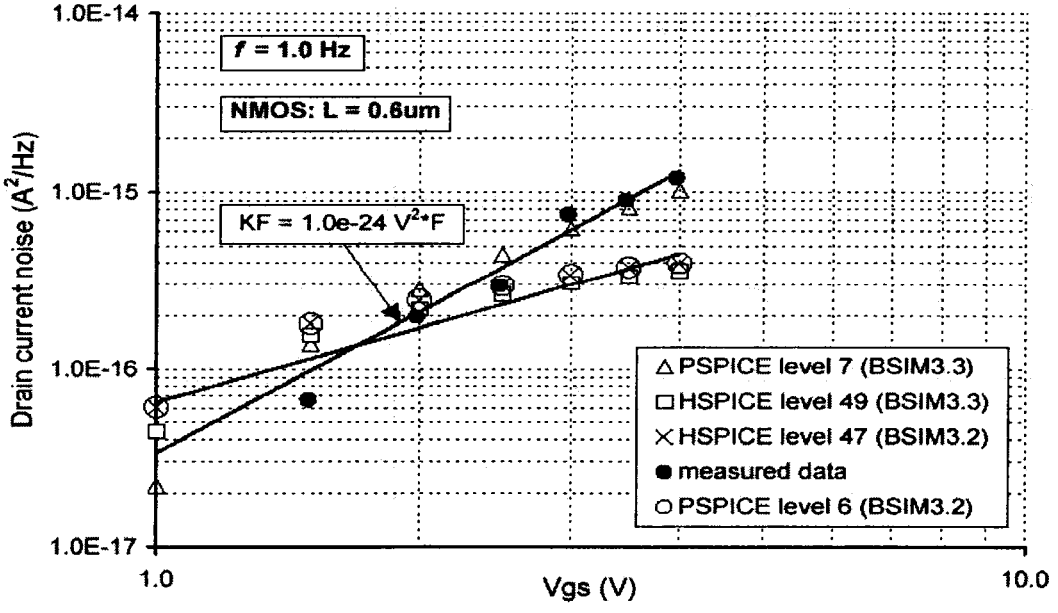

Figure 2.9. Different SPICE models used to simulated the drain current noise for the 0.6-um short channel NMOS transistors in the saturation region. $f = 1$ Hz.

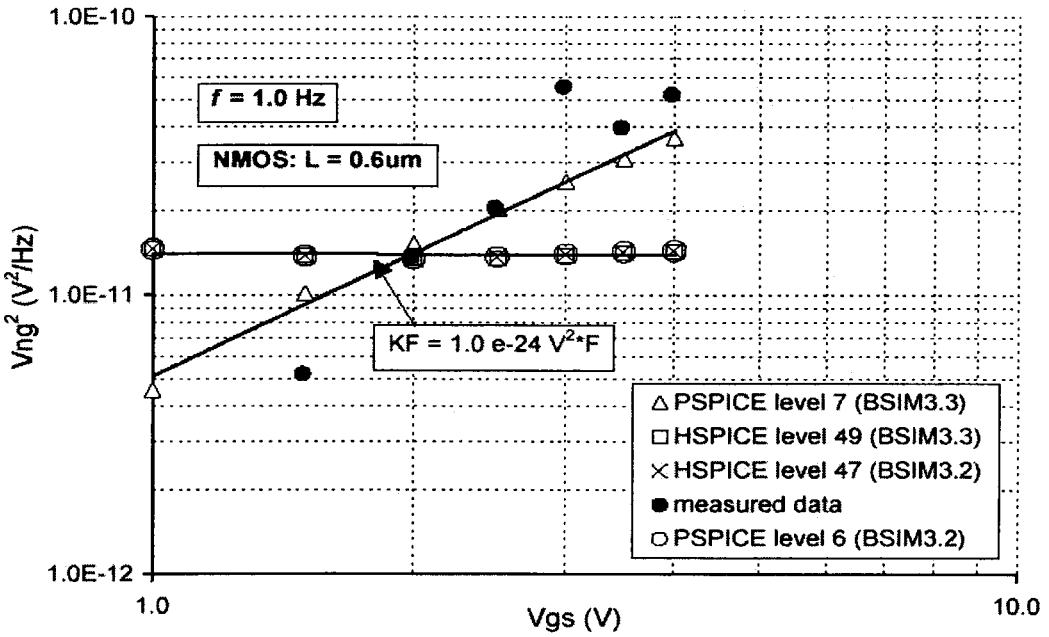

Figure 2.10. Different SPICE models used to simulated the input-referred voltage noise for the o.6-um short channel NMOS transistors in the saturation region. f = 1 Hz.

Fig. 2.11 shows some analog measurements of the input-referred voltage noise of NMOS transistors (L = 1.2 μm) at 1kHz in saturation region to determine the channel width effect. The tendency of noise to decrease with width, W, is consistent with the NLEV=3 or surface states model.

So, in conclusion, for NMOS devices in saturation region, the flicker noise is due to the number fluctuation, Eqn. 3 seems to be the most appropriate noise model to simulate the flicker noise for both long channel and short channel devices.

When in the subthreshold region (also called weak inversion), the gate potential applied in MOSFET (Vgs) is less than the threshold voltage (Vt), the channel charge and the depletion region charge in the MOSFET device are both affected by the applied gate

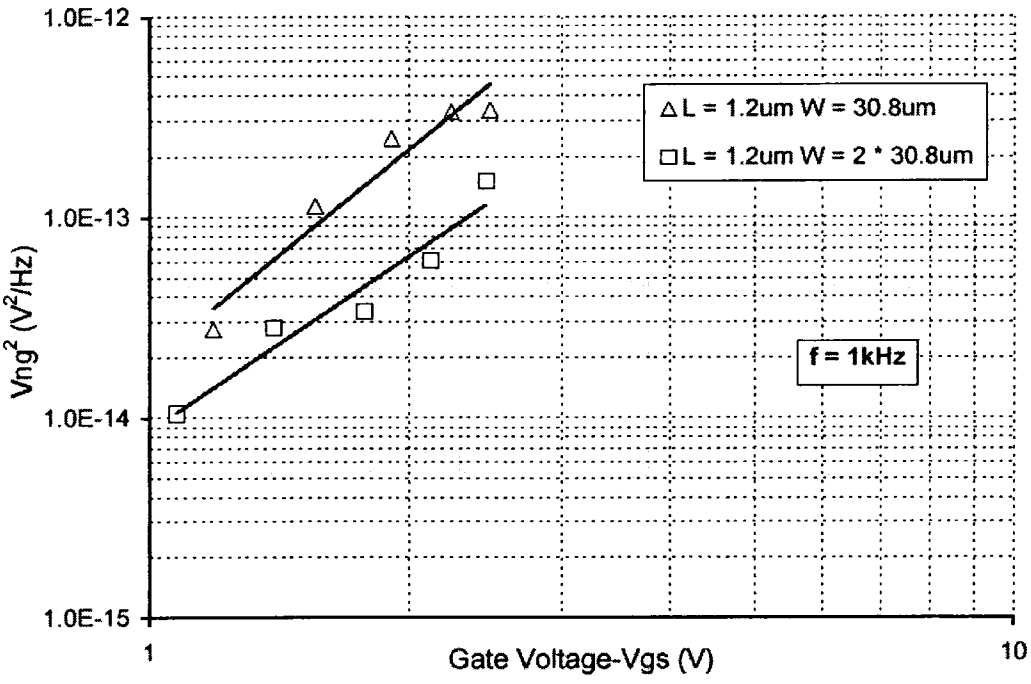

Figure 2.11. Analog measured 1.2-μm NMOS noise to determine channel width effect. W = 30.8 μm and W = 2 * 30.8 μm, at 1KHz in saturation region.

voltage [17]. The MOSFET transistor can thus work similar to a bipolar transistor because the electrons in the n^+ source region of an NMOS transistor can surmount the potential barrier to the p-type substrate and get into the channel region. Its characteristics can be defined as:

$$I_D = K_x \frac{W}{L} e^{V_{GS}/nV_T} (1 - e^{-V_{DS}/V_T})$$

So, the transconductance, gm, is an exponential function of gate voltage, Vgs, in subthreshold region, this will affect the input referred voltage noise a lot.

Fig. 2.12 shows the simulated and measured NMOS drain current noise versus absolute gate-source voltage in the subthreshold region for L = 5.0 μm, 1.2 μm and 0.6 μm respectively. Fig. 2.13 shows the corresponding simulated and measured NMOS input-referred voltage noise in the subthreshold region. The input referred voltage noise at the gate increases sharply as the gate voltage decreases drastically since the transconductance, gm, is an exponential function of gate voltage in subthreshold region. The level 3 model does not have an appropriate subthreshold model for long channel transistors, and the BSIM3.3 model also does not work for long channel devices, so no simulation can be done for 5-μm long channel devices. The BSIM 3.3 noise model in PSPICE level 7 does predict correctly the tendency of the change for the flicker noise.

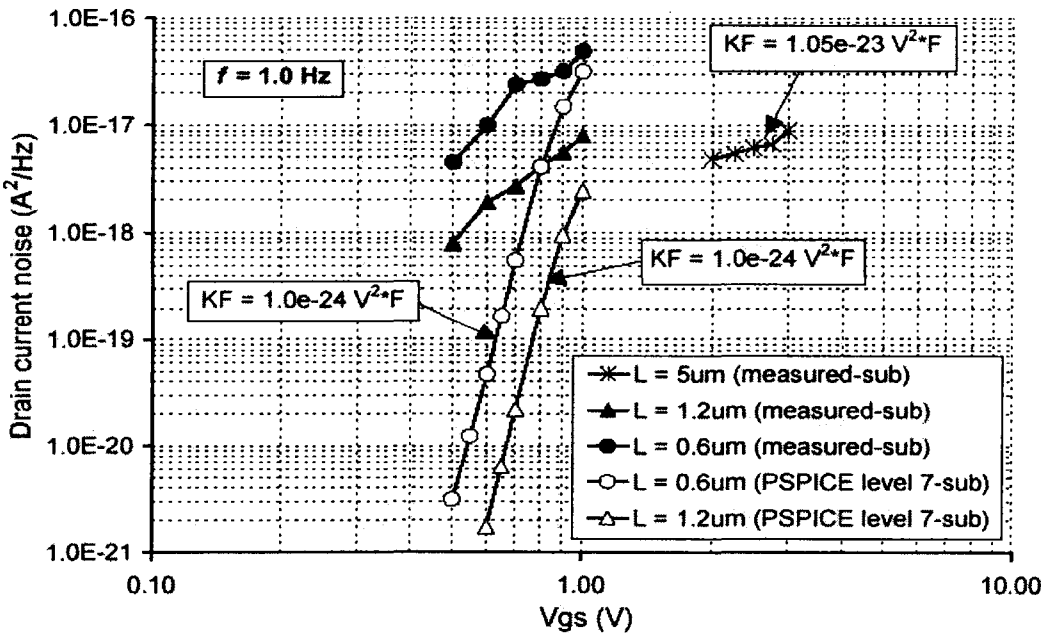

Figure 2.12. Simulated and measured NMOS drain current noise versus absolute gate-source voltage in the subthreshold region. L = 5.0 μm, 1.2 μm and 0.6 μm respectively. f = 1 Hz.

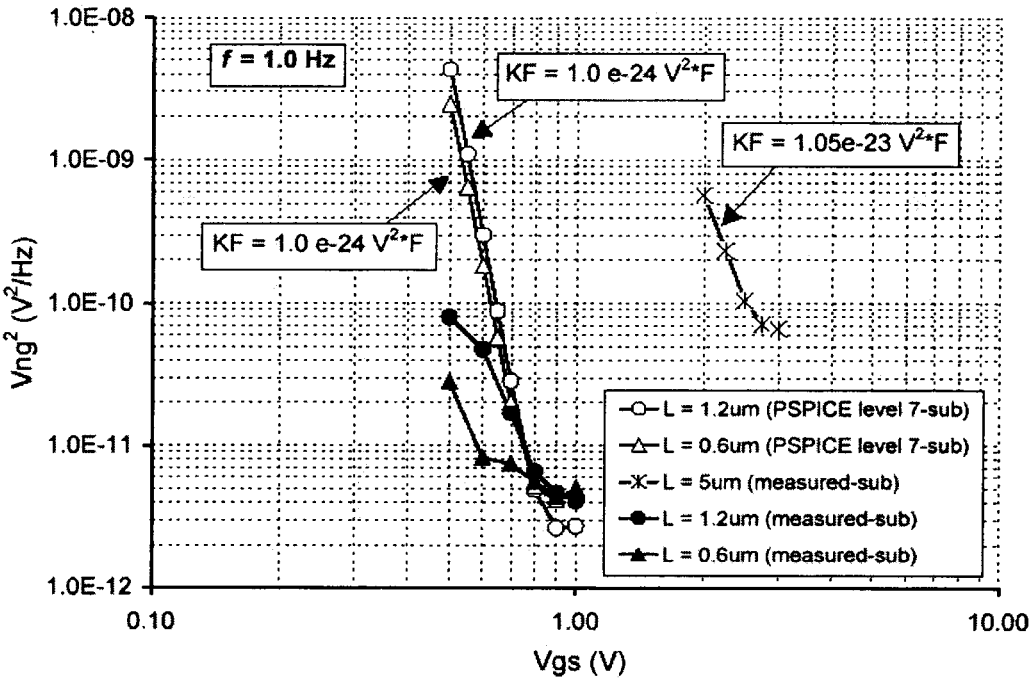

Figure 2.13. Simulated and measured NMOS input-referred voltage noise versus absolute gate-source voltage in the subthreshold region. L = 5.0 μm, 1.2 μm and 0.6 μm respectively. f = 1 Hz.

In conclusion, for NMOS devices in subthreshold region, the input referred voltage noise is larger than that of saturation region, and it decreases drastically when increasing the gate bias voltage. It seems that Eqn. 3 (NLEV=2 or 3) can still predict the noise tendency well for the short channel NMOS devices.

Fig. 2.14 and Fig. 2.15 give a summary of the results for both the input referred mean square noise voltage at the gate and the mean square drain current noise for both regions of operation and both types of devices. BSIM 3.3 here in both figures refers to PSPICE level 7.

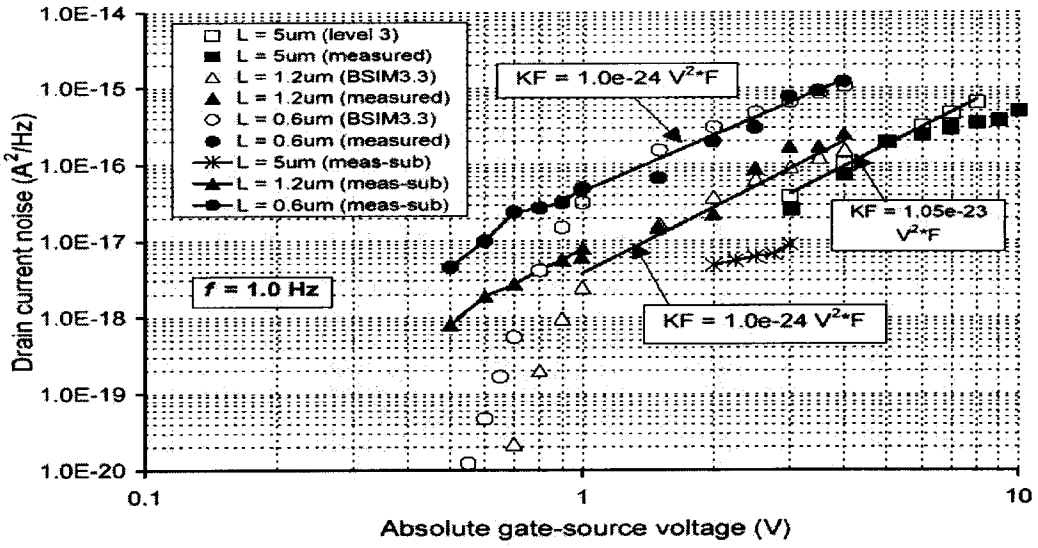

Figure 2.14. Summary of simulated and measured NMOS drain current noise versus absolute gate-source voltage from subthreshold to saturation region. L = 5.0 μm, 1.2 μm and 0.6 μm respectively. f = 1 Hz.

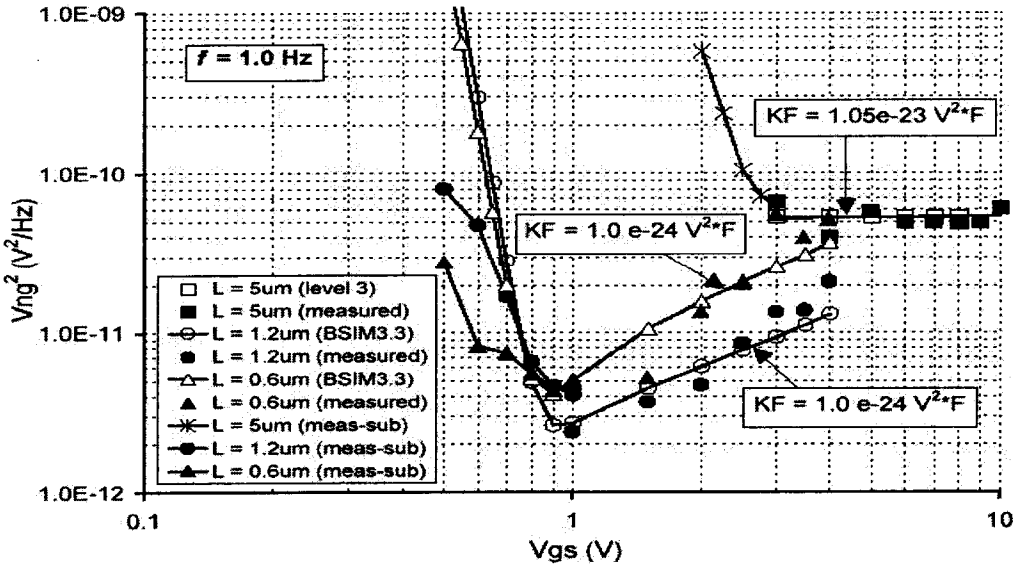

Figure 2.15. Summary of simulated and measured NMOS input-referred voltage noise versus absolute gate-source voltage from subthreshold to saturation region. L = 5.0 μm, 1.2 μm and 0.6 μm respectively. f = 1 Hz.

III. PHASE NOISE ON A 2-GHz CMOS LC OSCILLATOR

Most noise modeling in SPICE and other circuit simulators is accomplished only by using linearized AC models. The time varying nature of oscillators and large non-linearity's have precluded any meaningful application of techniques based on linear approximations, the simulations must be performed in the time domain. In this work we generate a pseudo-random noise with a $1/f$ power distribution and then sample this and inject it into SPICE as a piecewise linear waveform (PLW) in the time domain. An oscillator with this 1/f noise source is simulated in the time domain and a large number of points sampled in the time domain. This is then used to compute the fast Fourier transform (FFT) and find the spectra of the upconverted phase noise in the oscillator in the frequency domain. The simulation results are compared to the published experimentally measured data.

A. SIMULATION OF RANDOM-PHASE FLICKER NOISE

Based on our experimental results in Section II, we have found that for NMOS devices, the best model is obtained with NLEV = 2 or 3 and with AF = 1. We use then Eqn. 3 where NLEV = 2 or 3 and MATLAB to get the different values of flicker noise in a range of frequencies with a step frequency, fs. A larger than practical KF value can be used in MATLAB to accentuate the effects. This KF value is used for simulation of the current flicker noise, I_{flick}. The actual KF value representative of our simulated noise will be obtained after sampling the random-phase flicker noise, I_{flick}', in time domain and

using a fast Fourier transform (FFT). After obtaining the values of current flicker noise, I_{flick} (A/ $Hz^{½}$), from Eqn.6, we then calculate the amplitudes of current components associated with this, Iamp (A), by multiplying by the square root of fs.

$$Iamp = I_{flick} \cdot (fs)^{½} \tag{7}$$

An ideal sinusoidal current signal can then be expressed as

$$Ind(i) = Iamp(i) \cdot \sin[2\pi \cdot f(i)\, t + \Phi(i)] \tag{8}$$

Where $\Phi(i)$ is the random phase, f is frequency, i is the index of the frequency, which changes from 1 to the end of the frequency range used in the simulation.

The "rand" function in MATLAB is used to create a pseudo-random $\Phi(i)$, by using randomly created internal data in the computer. Then all the individual current components, Ind(i), are summed together to get the random-phase flicker noise, I_{flick}', in the defined frequency range.

$$I_{flick}' = \Sigma\, Ind(i), \qquad i = \text{range of the frequencies} \tag{9}$$

Fig. 3.1 is the simulation result for the flicker noise, I_{flick} , using KF = 1.0e-13 $V^2 \cdot F$, and using HSPICE NLEV = 2 & 3 or Eqn. (3) with AF = 1. The physical parameters for the NMOS transistors are: W = 400 μm, L = 0.7 μm, tox = 0.020 μm. The transconductance, gm, is 0.3 mA/ V according to our experiments.

Fig. 3.2 shows the amplitude of the current, Iamp, with different frequencies. In our simulation, the range of f is from 10 MHz to 1000 MHz with steps of 10 MHz (i.e. fs = 10 MHz).

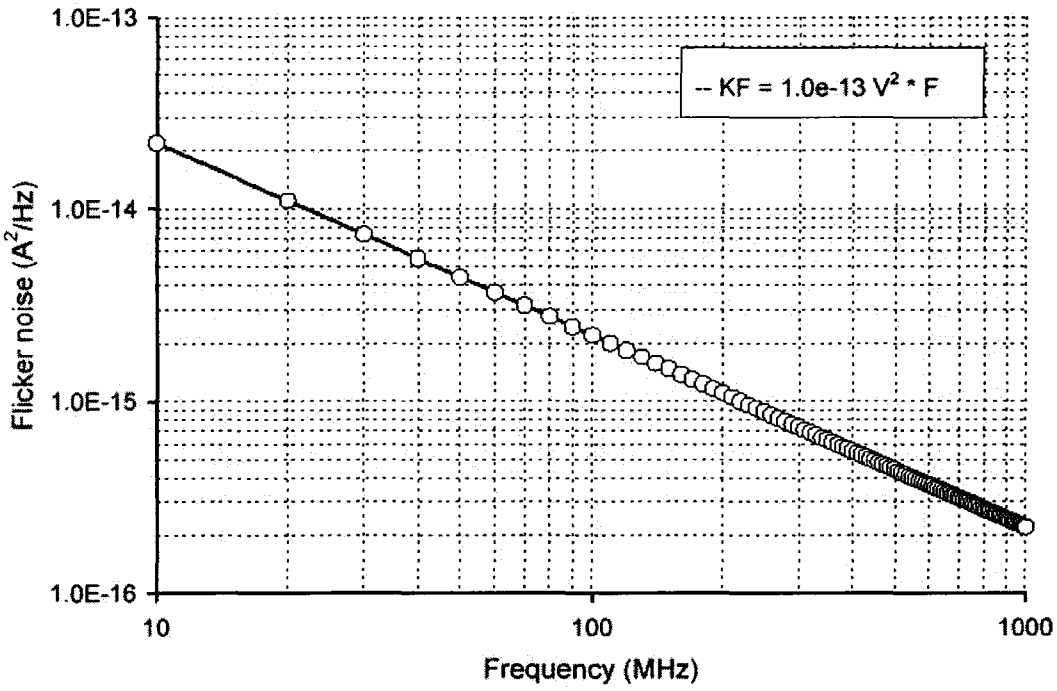

Figure 3.1. Modeled flicker noise with KF = 1.0e-13 ($V^2 \cdot F$).

Fig. 3.3 shows the sum of the individual current components to represent the flicker noise, I_{flick}'. The time domain is shown in steps of 100 ps for a total of 0.1 μs in the simulation. This I_{flick}' signal is then sampled in steps of 100 ps again in the time domain and transformed to the frequency domain by FFT.

The result of FFT is plotted as Fig. 3.4, to get the actual value of KF corresponding to the random-phase flicker noise. According to Eqn.3 and because I_{flick} in Eqn.3 represents the peak amplitude, hence, $I_{flick}^2 / 2 = i_n^2 / \Delta f$ is the power spectral density. The actual KF value obtained for the simulated noise in Fig. 3.4 was KF= 1.0e-13 $V^2 \cdot F$, which is very close to or the same as the KF value used in the beginning to simulate the flicker noise.

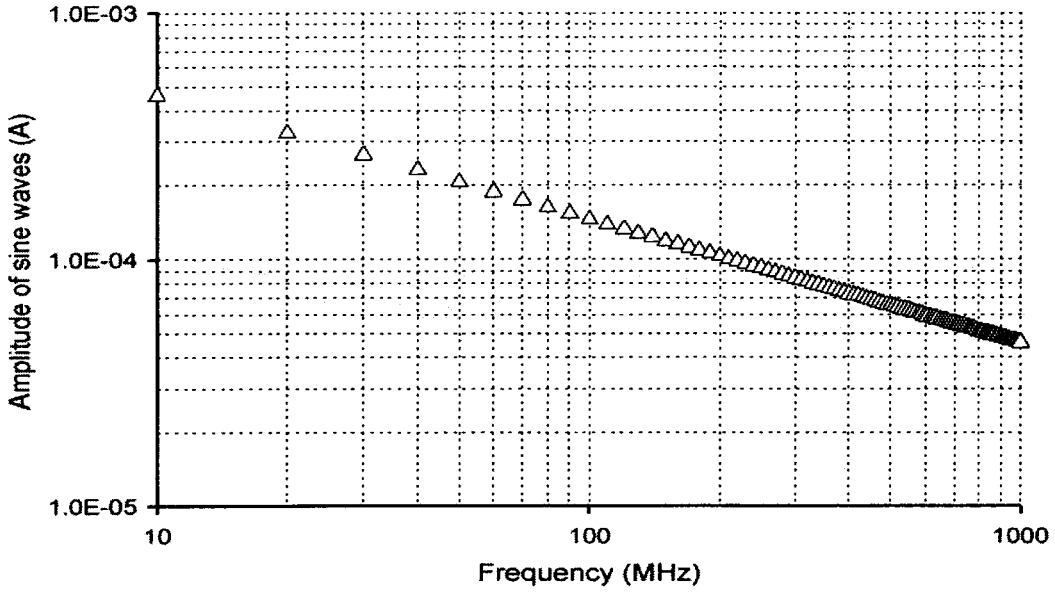

Figure 3.2. Calculated amplitude of sine waves when KF = 1.0e-13 ($V^2 \cdot F$).

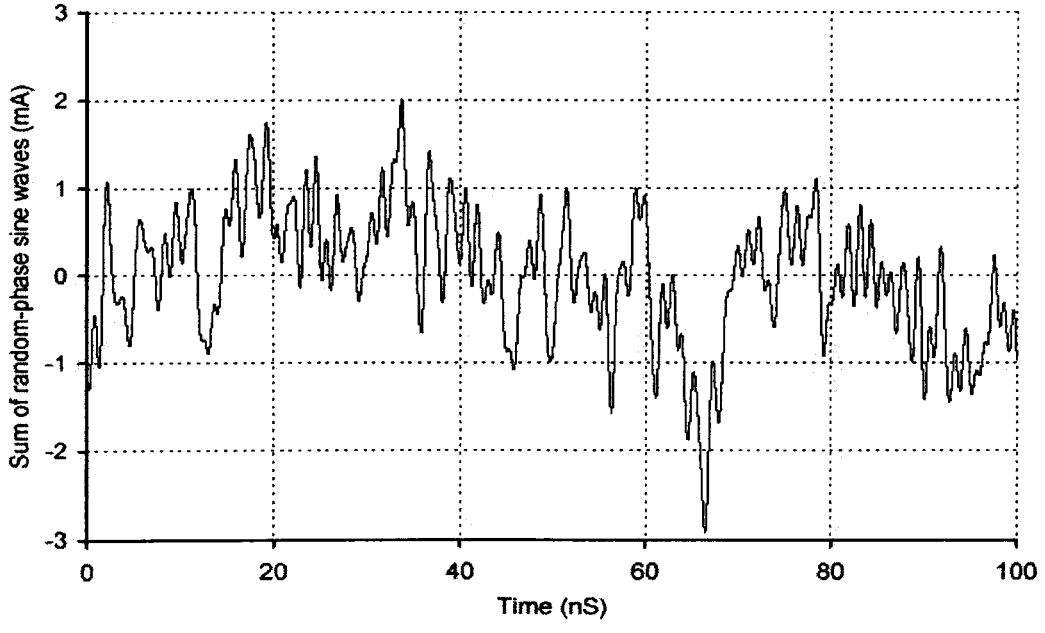

Figure 3.3. Sum of sine waves with random phase when KF = 1.0e-13 ($V^2 \cdot F$).

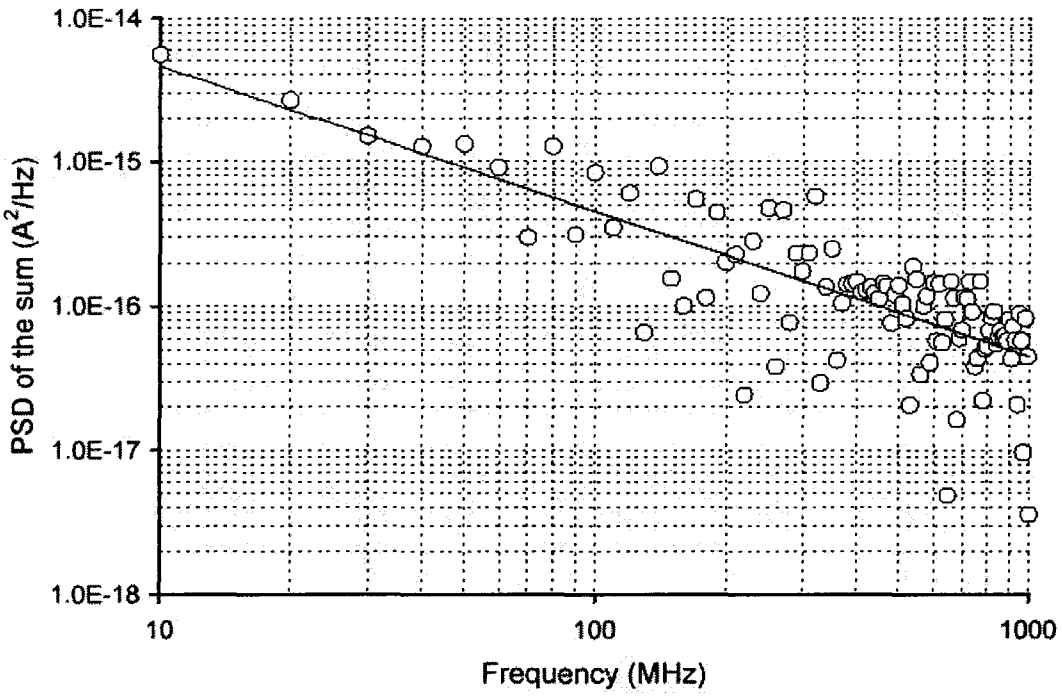

Figure 3.4. Power spectral density of the sum of sine waves with random phase. The original KF value is KF= 1.0e-13 ($V^2 \cdot F$).

B. SIMULATION OF PHASE NOISE EFFECTS ON LC OSCILLATOR

A low phase noise cross-coupled LC CMOS VCO shown in Fig. 3.5 similar to that in reference [44] has been simulated. All of the dimensions are shown in the figure. The random-phase flicker noise, I_{flick}', is injected into the signal path as a piecewise linear waveform at the drain of one of the differential pairs, here it is M2 an NMOS transistor.

The internal FFT function in HSPICE is used to compute the FFT of HSPICE simulation output in the time domain. To get the sharpest and best figure, a Blackman-Harris window is used with 2048 points, NP=2048, in the FFT analysis.

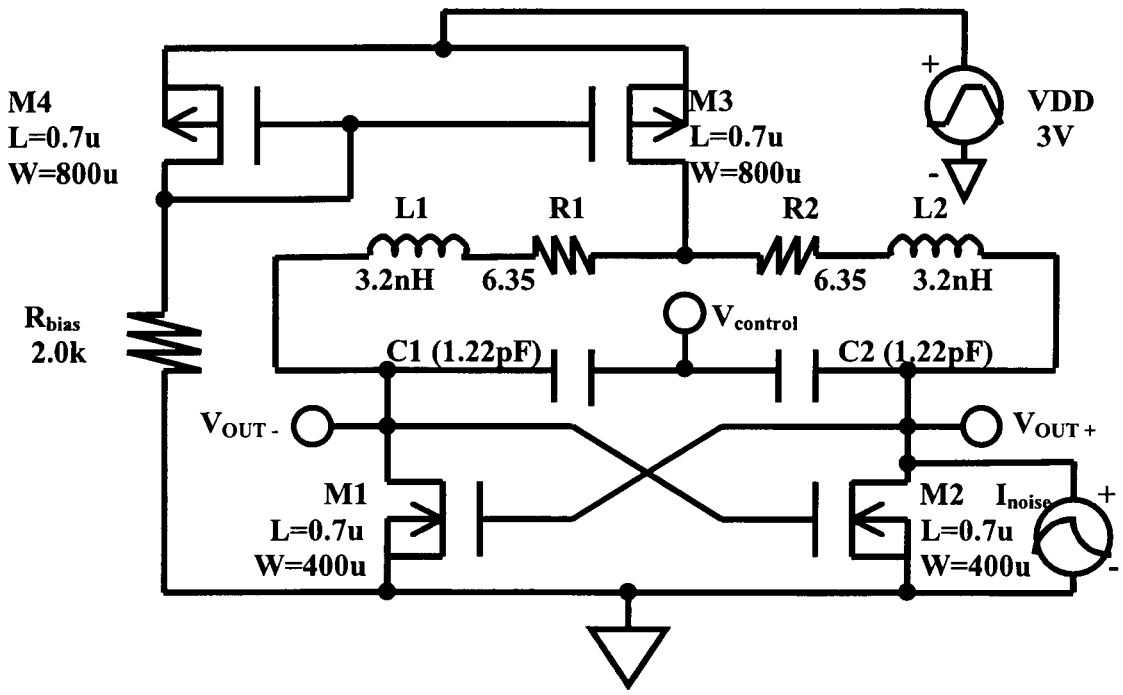

Figure 3.5. LC CMOS oscillator circuit for simulation

Five different conditions of random-phase flicker noise, including one without added noise, are applied to the LC oscillator. These correspond to five different KF values. Fig.3.6 shows these HSPICE simulation results. The carrier frequency of the LC oscillator is 2.0 GHz. When there is no added phase noise, there are sideband harmonics with large peaks. As the added phase noise becomes larger due to larger KF values, these harmonics are gradually hidden, and the power in the output at frequencies where there are no harmonics becomes larger. This tendency is shown much more clearly in Fig. 3.7, which shows the effect of KF at fm = 1.2 GHz and fm = 1.5 GHz respectively.

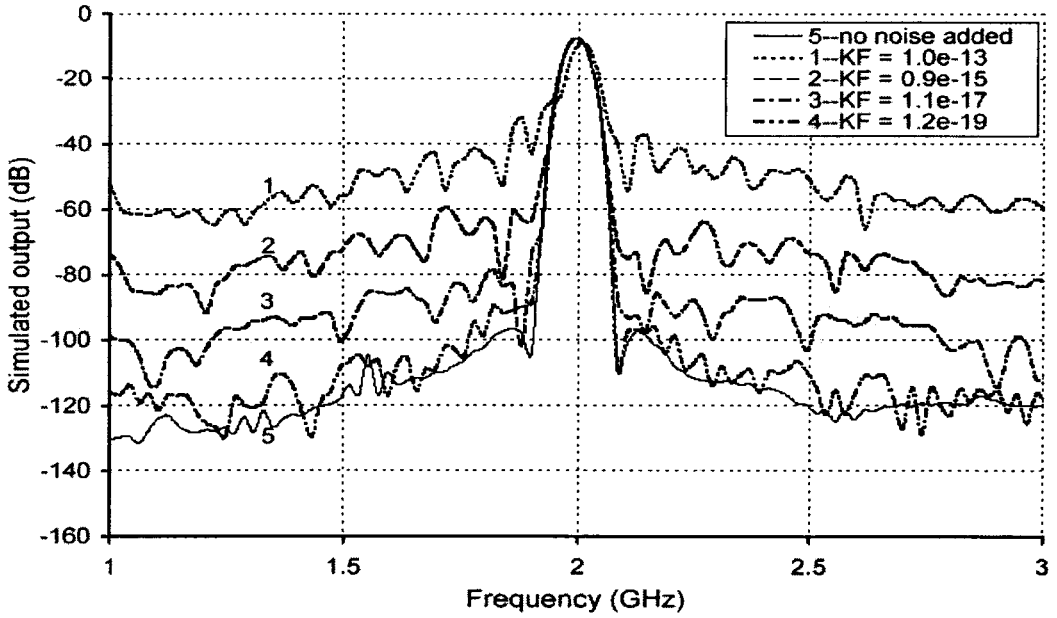

Figure 3.6. Simulated output power spectra of LC oscillator under different KF values, f_0 = 2.0 GHz.

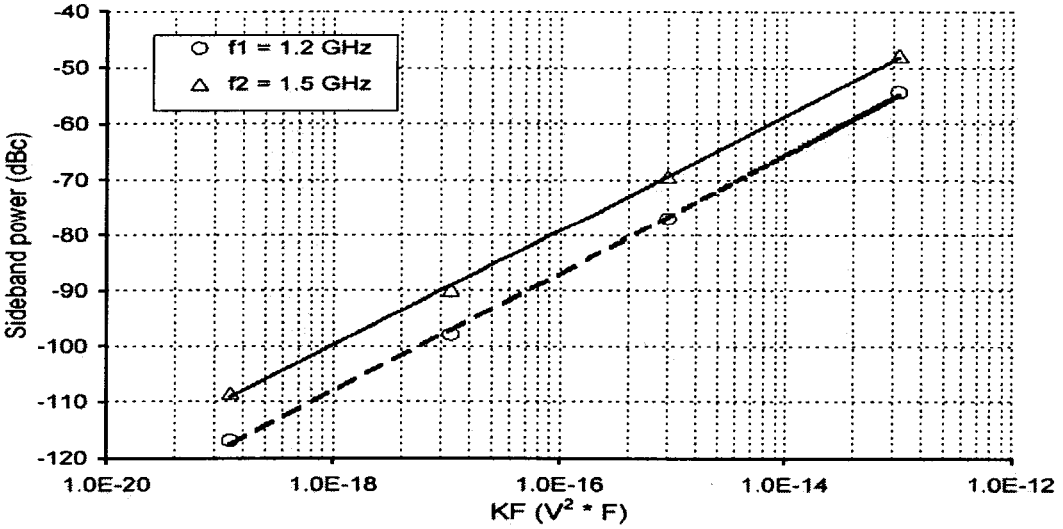

Figure 3.7. Simulated sideband power versus KF value for frequencies below carrier, f_0 = 2.0 GHz.

Fig. 3.8 shows the sideband phase noise power spectra for the five different KF values. The theory of conversion of flicker noise to phase fluctuations and phase-noise sidebands predicts a $1/f^3$ dependency for the phase noise spectrum [43]. The amplitude of low frequency flicker noise is determined by the coefficient *Co* and has a $1/f^3$ dependence on the offset frequency. In Fig. 3.8, we can see this theory is proven to be correct, and no $1/f^2$ portion could be found in Fig. 3.8.

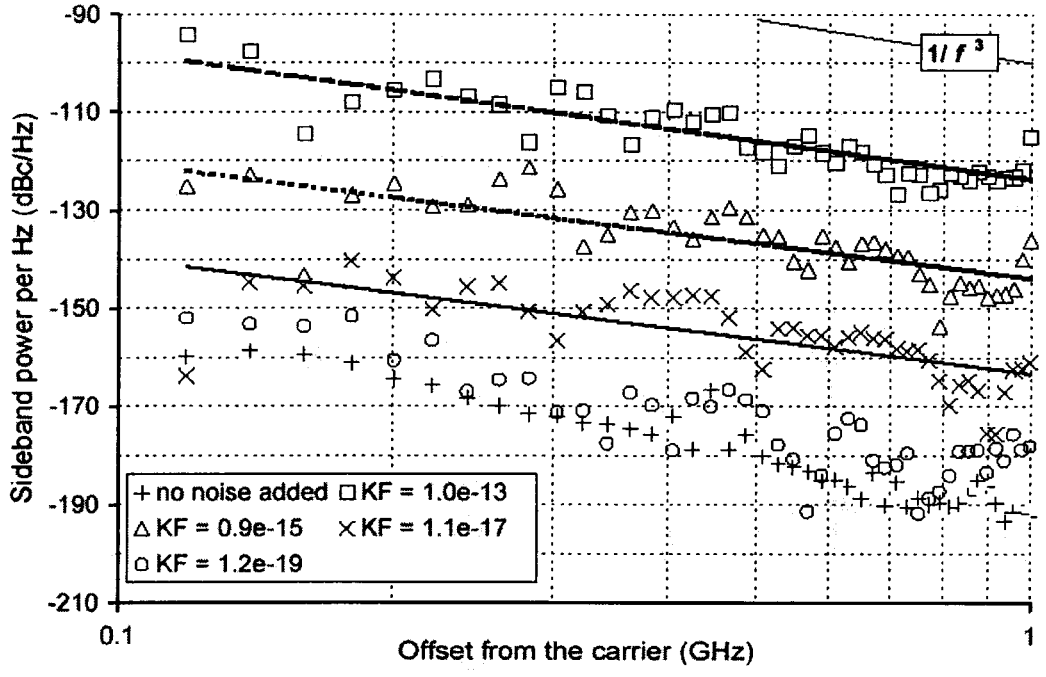

Figure 3.8. Simulated sideband power versus offset from the carrier with different KF values, f_0 = 2.0 GHz.

According to Eqn. 6, in the $1/f^3$ portion of the phase noise spectrum, the phase noise sideband PSD can be simply related to the KF value by:

$$L\{\Delta f\} = 10 \cdot \log (CF \cdot KF / \Delta f^3) \qquad (10)$$

where CF is the empirical coefficient. This follows since the KF value is proportional to the $1/f$ noise corner frequency, $\omega_{1/f}$.

The simulation results in Fig. 3.8 show that for an offset frequency of Δf = 100 MHz, when KF is 1.0e-13 $V^2 \cdot F$, then $L\{100\ MHz\}$ = -97.9 dBc/Hz, which then yields CF = 1.6e27 from Eqn. 10. At the same offset frequency, when KF is 1.1e-17 $V^2 \cdot F$, $L\{100$ MHz$\}$ = -139.8 dBc/Hz, which yields CF = 0.9e27 from Eqn. 10. These two CF values are very close to each other, which verifies the empirical formula. We can also see that the expected difference for the sideband power per unit frequency at a 100 MHz offset, L(100 MHz), using the two different KF values, is 40.5 dB/Hz. The simulation results give 41.9 dB/Hz for the difference, the error is only 1.4 dB/Hz.

Applying the average CF value, 1.3e27, and our experimental KF value, 1.0e-21 $V^2 \cdot F$, which was obtained for the 0.7-μm NMOS transistors from our measurements, then at an offset of Δf = 600 kHz, Eqn. 10 predicts $L\{600\ kHz\}$ = -112.2 dBc/Hz. This is in good agreement with a measured value of –116 dBc/Hz, given in reference [44].

Fig. 3.9 shows some of the measured and the simulated sideband phase noise power values. They match each other well if considering that in our simulation, only the flicker noise in the drain of the NMOS transistor is injected, while the measured data comes from the whole CMOS LC oscillator which include two more PMOS transistors. Our simulations are so shown to be able to predict the phase noise correctly.

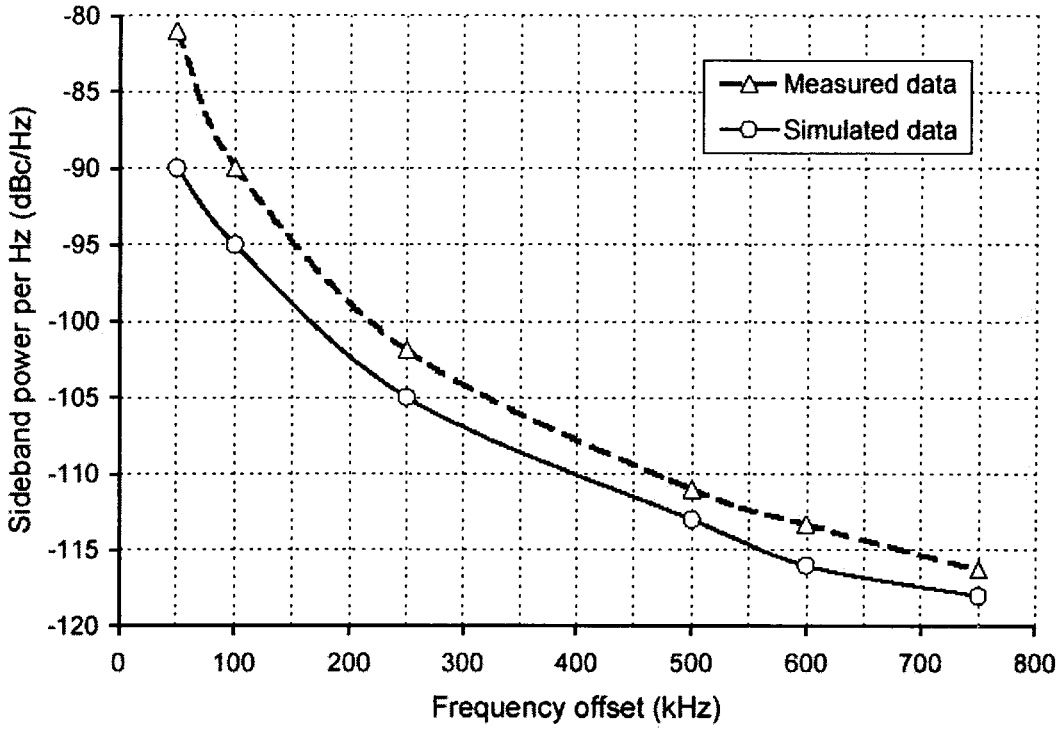

Figure 3.9. Comparison of the simulated sideband power with the measured sideband power, f_0 = 2.0 GHz.

C. RESULTS AND DISCUSSIONS

Flicker noise has been simulated as a sum of sine waves with different amplitudes and random phases in MATLAB, which is shown to have a $1/f$ power distribution characteristic after FFT. The actual KF value corresponding to this sum of sine waves can then be made close to the experimental KF values. Inserting this flicker noise into a LC oscillator results in it being up-converted to phase noise.

The HSPICE simulation results clearly show that the phase noise of the 2-GHz LC oscillator proportionally becomes large as the KF value increases, and supports the

empirical theory giving the $1/f^3$ dependence for the phase noise spectrum, which is due to the up-converted $1/f$ flicker noise.

The phase noise sideband power spectral density predicted by simulation corresponds well with the measured noise value in the literature where the 2-GHz LC oscillator has same structure if considering that in our simulation, only the flicker noise in the drain of one of the two NMOS transistor is injected, while the measured data comes from the whole CMOS LC oscillator which includes two more PMOS transistors.

IV. CONCLUSION AND FUTURE WORK

A. CONCLUSION FOR NMOSFET NOISE

For long channel NMOS (L = 5 μm) devices, the input-referred gate-voltage noise (Vng^2) is independent of gate bias (Vgs), which shows the surface state model and the noise model (NLEV = 2 and 3) in SPICE is more appropriate. SPICE device model level 3 and noise model NLEV 2 & 3 can predict the long channel NMOS noise performance very well in saturation region, but not in subthreshold region, and also cannot be used to simulated the short channel NMOS noise performance.

For short channel NMOS devices (L = 0.6 μm and 1.2 μm), the input-referred gate-voltage noise (Vng^2) is dependent on gate-source voltage (Vgs), increasing proportionally as Vgs increase, which is due to the nonlinearity of the transconductance (gm) variation with gate bias. These devices can be modeled with the BSIM 3.3 device model (level = 7 in PSPICE) and the same noise model (NLEV = 2 and 3) in SPICE is also appropriate. BSIM 3.3 in PSPICE can predict the short channel NMOS noise performance in both the saturation and the subthreshold region, but does not work for long channel NMOS devices. There appears to be an error in the HSPICE BSIM 3.3, level 49, equations for input referred noise voltage. HSPICE does however correctly model the mean square drain current noise.

Flicker noise has been simulated as a sum of sine waves with different amplitudes and random phases in MATLAB, which is shown to have a $1/f$ power distribution characteristic after FFT. The actual KF value corresponding to this sum of sine waves

can then be made close to the experimental KF values. Inserting this flicker noise into a LC oscillator results in it being up-converted to phase noise.

The HSPICE simulation results clearly show that the phase noise of the 2-GHz LC oscillator proportionally becomes large as the KF value increases, and supports the empirical theory giving the $1/f^3$ dependence for the phase noise spectrum, which is due to the up-converted $1/f$ flicker noise. The phase noise sideband power spectral density predicted by simulation corresponds well with the measured noise value in the literature where the 2-GHz LC oscillator has same structure.

Adoption of these techniques will allow the design of oscillators which minimize phase noise.

B. FUTURE WORK

We have done some measurements on the flicker noise in long channel (5-ìm) and short channel (2.4-ìm, 1.2-ìm and 0.6-ìm) p-MOSFET's in saturation region. Fig. 4.1 and Fig. 4.2 show the measured 5-μm PMOS mean square drain current noise and input-referred voltage noise in saturation region respectively. From Fig. 4.1, we can have

$$\overline{I_{nd}^{\,2}} \propto \frac{I_{ds}}{L^{\alpha} f}$$

where α is close to 2, and which is very likely to be the Eqn. 1 (NLEV = 0). That is because the drain current noise in Fig. 4.1 is proportional to the drain current, and the 2-parallel-PMOS (i.e., L/(2*W)) device has almost the same drain current noise as the

single-PMOS device (i.e., L/W), and both of them have about 2-3 time large noise as the 2-series-PMOS device (i.e., (2*L)/W).

In saturation region, it can be readily shown from the above relationship that:

$$\overline{V_{ng}^{\,2}} = \frac{\overline{I_{nd}^{\,2}}}{g_m^{\,2}} \propto \frac{1}{WLf}$$

Fig. 4.2 just shows that this relationship is true, where the 2-series-PMOS device has almost the same noise power as the 2-parallel-PMOS device. However, the input-referred voltage noise (Vng2) in Fig. 4.2 is also proportional to the effective gate voltage ($V_{GS}^* = |V_{GS}| - |V_T|$), which the Eqn. 1 (NLEV = 0) does not predict.

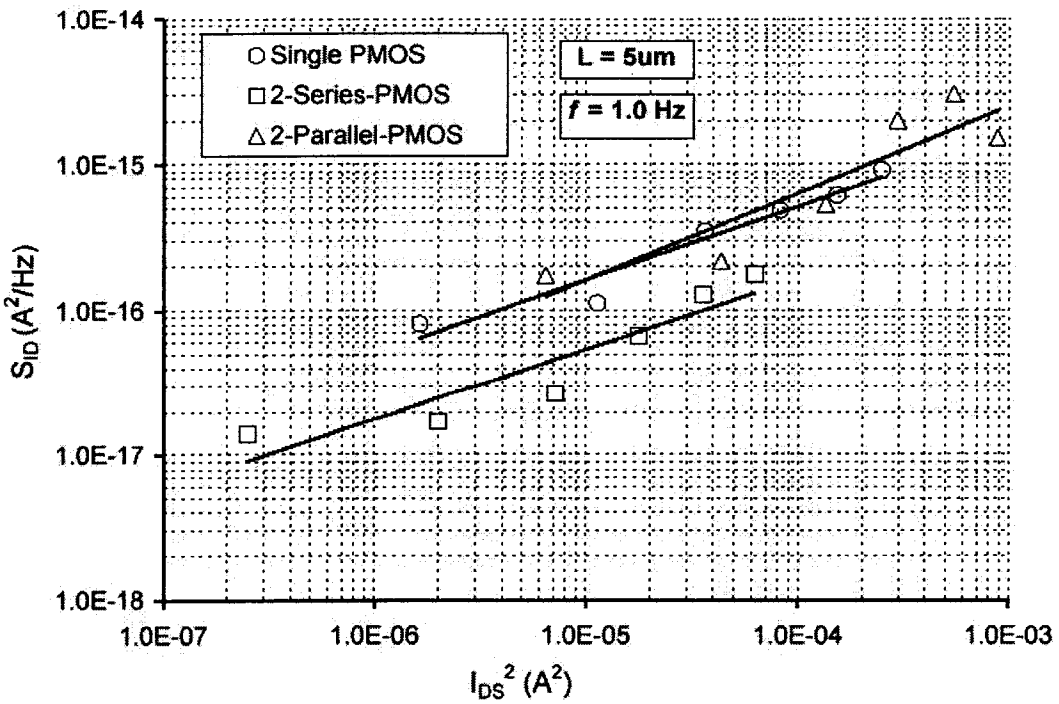

Figure 4.1. Measured PMOS drain current noise versus drain current square in the saturation region. L = 5.0 μm W = 120 μm for a single PMOS device. f = 1 Hz.

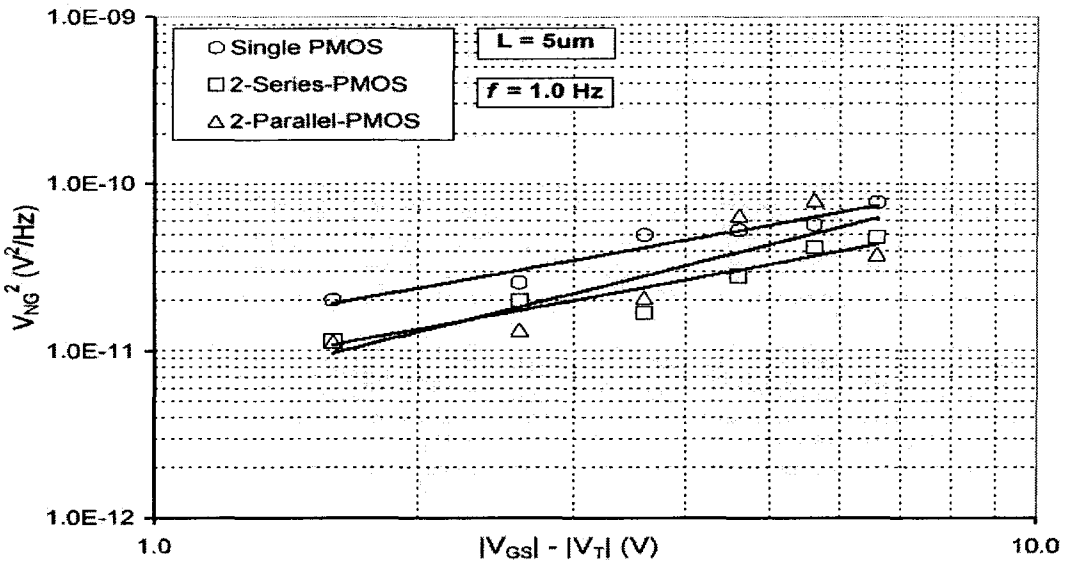

Figure 4.2. Measured PMOS input-referred voltage noise versus effective gate voltage in the saturation region. L = 5.0 μm W = 120 μm for a single PMOS device. f = 1 Hz.

The short-channel PMOS noise measurement results are shown in Fig. 4.3 and Fig 4.4. We cannot tell which noise model is more appropriate to match them.

So some work could be done for the future research in the PMOS noise area:

♦ Double-check the long channel PMOS (5-μm) noise figure, and try to simulate the measurement results by using SPICE noise model (NLEV=0).

♦ More research on the short channel PMOS noise figure, including finding out a better noise model by doing some fundamental theory research and simulation.

♦ Phase noise research: inject the PMOS flicker noise into the 2-GHz CMOS LC oscillator using HSPICE, to see a better match effect between the simulation results and the published data.

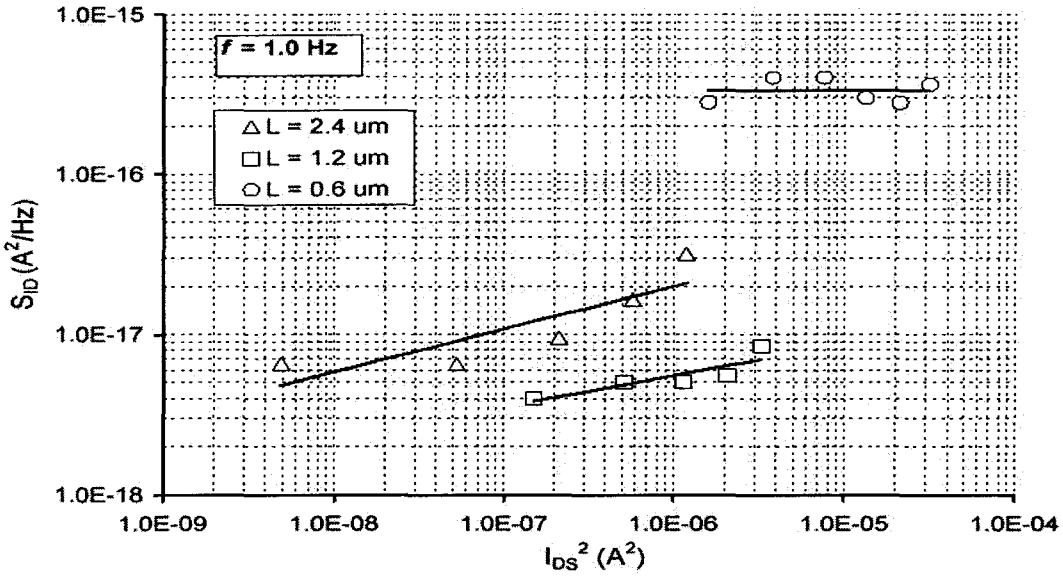

Figure 4.3. Measured sub-micron PMOS drain current noise versus drain current square in the saturation region. L = 0.6 μm, 1.2 μm and 2.4 μm. f = 1 Hz.

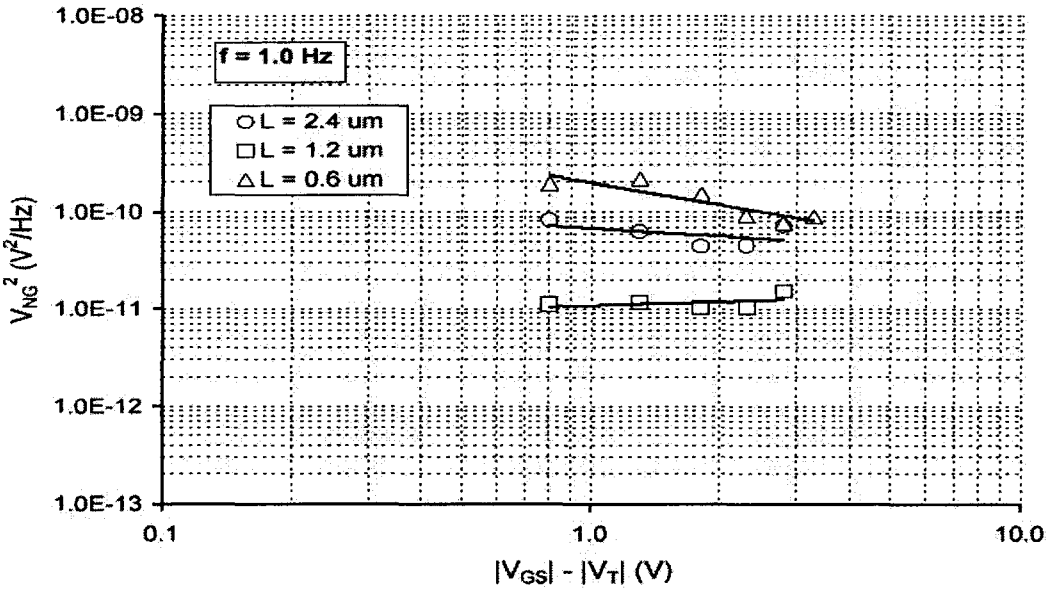

Figure 4.3. Measured sub-micron PMOS input-referred voltage noise versus effective gate voltage in the saturation region. L = 0.6 μm, 1.2 μm and 2.4 μm. f = 1 Hz.

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APPENDIX

The following programs have been used in this research to deal with the measured noise data and the SPICE simulations.

1. MATLAB Program A

This program collects the Digital Multimeter (DMM) data, which is in the form of voltage variation (unit, V) at the drain of the NMOS transistor in time domain, and then changes it to the drain current noise (A^2/Hz) by doing the fast Fourier transform (FFT). The results were plotted in frequency domain ranging from about 0.01 Hz to 4.2 Hz. Then the average drain current noise at the 1.0 Hz of frequency was obtained by reading from the figure. There are some notes in the program to help to understand the program.

```
% PSD of nmos 1/f noise
% data is taken from experimental research lab

clear all; close all

load 'N106t1a7.dat'    % NMOS data from Digital Multimeter

Vout = n106t1a7;       % Unit = V
date = '4/29/99';      % the date when data is taken

fs=26;                 % the sampling rate of DMM
gain=90;               % noise amplification ratio by LM741
Rload=100;             % load resistor
Vnoise = Vout./gain;   % NMOS drain voltage noise (V)
Inoise = ( Vnoise./Rload);   % NMOS drain current noise (A)
L = length(Inoise);    % L is also a window size. As L get
                       % larger, the magnitude of fft gets
                       % closer to theoritical val

%SETUP AXIS
f = fs .* ( 0:1/L:1-1/L );     % up to f=fs (Hz)
f = f(1:L/2);                  % up to fs/2
time=(0:L-1)/fs;               % unit = S
```

```
%PSD of NOISE
mag = (1/(L*fs))*abs( fft(Inoise) ).^2; % unit = A^2/Hz
mag = mag(1:L/2);              % the desired mean square
                               % drain current noise

figure(1);                     % two figures in one page

subplot(2,1,1);
        % DMM output in time domain (Fig. 2.2 in the thesis)
   plot(time,Vout); grid on;
   axis([0,200,-0.024,-0.018]);  % axis need to adjust
   title(sprintf('%s (%d pts, %s)',L,date));
   xlabel('Time (S)');           % label of the X axis
   ylabel('DMM output (V)');     % label of the Y axis
   zoom on

subplot(2,1,2);
        % measured mean square drain current noise in
        % frquency domain (A^2/Hz)
   loglog(f,mag,'r'), hold on, grid on,
   axis([0.01,10,1e-20,1e-13]);          %axis need to adjust
   title('PSD of NMOS Darin Current Noise (A^2/Hz) at
          Vgs=2.5v');
   xlabel('Frequency (Hz)');
   ylabel('PSD of NMOS drain current noise (A^2/Hz)');
   hold on,
   loglog(f,1e-16./f.^1,'b-.'),              % 1/f noise line
   zoom on

   gm = 3.9e-3;      % measured when Vgs = 4 V for 5-um NMOS
   mag1 = mag./gm.^2;  % change to input-referred noise

figure(2);
        % measured input-referred voltage noise in frequency
        % domain (A^2/Hz)(Fig. 2.3 in the thesis)
   loglog(f,mag1,'r'), hold on, grid on,
   axis([0.01,10,1e-14,1e-7]);          %axis need to adjust
   title('Power spectral density (PSD) of measured NMOS
         input-referred noise.');
   xlabel('Frequency (Hz)');
   ylabel(Measured NMOS noise (V^2/Hz)');
   hold on,
   loglog(f,3e-11./f.^1,'b-.'),  % 1/f noise line
   zoom on

HOLD OFF
```

The following figures show the DMM output (before being amplified) and the measured background noise for the automated system. From Figure A.2, we can determine that at the frequency of 1.0 Hz, the background noise is about 4.0e-18 V^2/Hz.

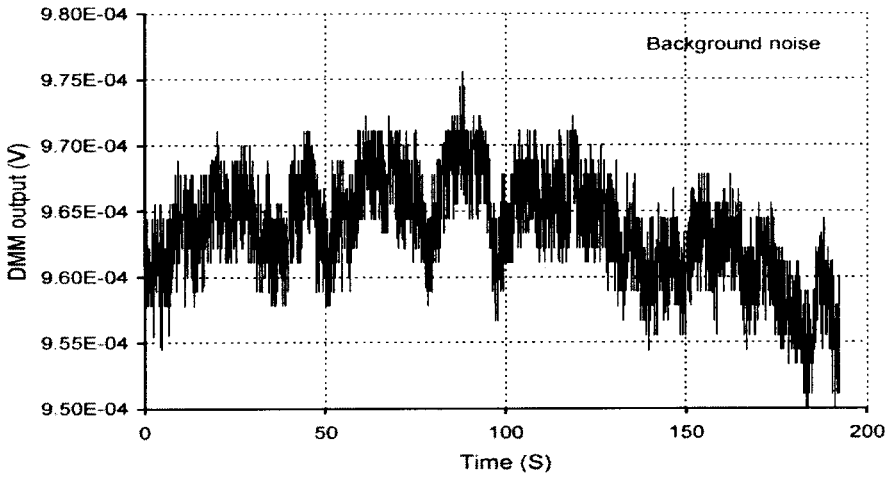

Figure A.1. Digital Multimeter output in time domain for automated system background.

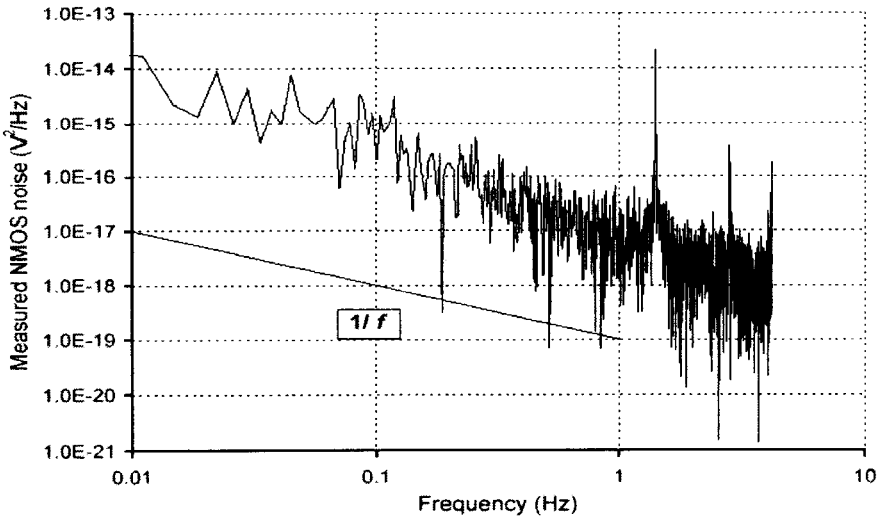

Figure A.2. Power spectral density (PSD) of measured background noise

2. PSPICE level 7 Simulation Program for flicker noise

This program is used to simulate the 0.6-um NMOS flicker noise by PSPICE level 7 (BSIM 3.3). First of all, the transistor DC characteristics, including the drain current, Ids, and the transconductance, gm, are matched to the experimental measured data by adjusting the parameters in the PSPICE models, such as the oxide thickness, TOX, and the intrinsic transconductance parameter, KP. After that, the noise characteristics can be simulated according to the noise experimental results using the appropriate noise equation selector (NLEV, or NOIMOD), flicker noise exponent (AF) and coefficient (KF) in PSPICE.

The output file of the PSPICE simulation does not directly give the mean square drain current noise (Ind^2) and the input-referred voltage noise (Vng^2). It gives the value of FN (output flicker noise at the drain node, V^2/Hz). We can calculate the drain current noise and the input-referred voltage noise by the following:

$$\overline{I_{nd}}^2(A^2/Hz) = \frac{FN(V^2/Hz)}{Rload^2(\Omega^2)}$$

where Rload is the drain load resistance. In our case, its value is 100 ohms,

$$\overline{V_{ng}}^2(V^2/Hz) = \frac{\overline{I_{nd}}^2(A^2/Hz)}{g_m{}^2(1/\Omega^2)}$$

and where gm can be obtained directly from the output file of the PSPICE simulation.

```
NMOS Noise Simulation L=0.6um level 7 in PSPICE (BSIM 3.3)

VDD 3 0 dc=5V          % DC power supply at the drain node
VGS 1 0 dc=2V ac=1V    % DC, AC power supply at the gate node
Rg 1 2 1K              % resistive load at the gate node
```

```
Rd 3 4 100              % resistive load at the drain node
Cgs 2 0 100u            % additional gate-source capacitance

m1 4 2 0 0 ntran l=0.6u w=30.8u                % NMOS netlist

.MODEL ntran NMOS level=7 tox=95.0e-10 vto=0.7v kp=50e-06
                  % main parameters of DC characteristics

*+ nlev=3 af=1 kf=1.0e-24     % noise model parameters
+ af=1 kf=1.0e-24 noimod=1    % in PSPICE level 7, the
                              % default value of noimod is 1

.ac dec 100 .01 2             % AC analysis
.NOISE V(4,0) VGS 10          % noise analysis
.dc VGS 1 4 0.5               % DC analysis
.probe                % write all analysis data to output file
.op                   % calculate and print all dc node
                      % voltages and voltage source currents

.END                  % end of PSPICE simulation input file
```

We also list all the device models and the noise models used in this thesis work for the simulation of NMOS transistors in Table A.1, which is the same as Table 2.1. According to our simulation and measured results, we believe there is an error in the BSIM 3.3 manual, where it refers the noise equation selector, NOIMOD = 1, to the noise equation, NLEV = 0. We think the NOIMOD =1 should refer to the noise equation, NLEV = 2 & 3. The detailed explanation is as following:

For example, the parameters for the 0.6-μm NMOS transistor used in simulation are: TOX = 95e-10 m, KF = 1.0e-24, L = 0.6 μm, W = 30.8 μm.

When Vgs = 2.0 V, the simulated DC characteristics are:

Ids = 3.29e-3 A, gm = 4.019e-3 Simens.

At frequency of 1.0 Hz, the simulated drain current noise, upon setting the noise equation selector, NOIMOD = 1, is: Ind^2 = 2.171e-16 A^2/Hz.

Now let's calculate the mean square drain current noise using the noise equations provided in SPICE, NELV = 0 and NELV = 2 & 3:

For NLEV =0,

$$\overline{I_{nd}^{\ 2}} = \frac{KF \bullet I_{ds}^{\ AF}}{C_{OX} \bullet L_{eff}^{\ 2} \bullet f} = \frac{(1.0e-24)\times(3.29e-3)^{1}}{(3.63e-3)\times(0.6e-6)^{2}\times 1}\frac{A^2}{Hz} = 2.51\times 10^{-12}\frac{A^2}{Hz}$$

For NLEV = 2 & 3,

$$\overline{I_{nd}^{\ 2}} = \frac{KF \bullet g_m^{\ 2}}{C_{OX} \bullet W_{eff} \bullet L_{eff} \bullet f^{AF}}$$

$$= \frac{(1.0e-24)\times(4.019e-3)^{2}}{(3.63e-3)\times(0.6e-6)\times(30.8e-6)\times 1}\frac{A^2}{Hz} = 2.56\times 10^{-16}\frac{A^2}{Hz}$$

So, by comparing with these three drain current noise values, we find that the drain current noise simulated by PSPICE level 7 (BSIM 3.3) with NOIMOD = 1 is almost the same as the one calculated by using NLEV =2 & 3 noise equation, and they are both much smaller than that one calculated from the noise equation, NLEV = 0.

In other words, NOIMOD =1 in PSPICE level 7 (BSIM 3.3) should refer to the noise equation, NLEV = 2 & 3, not NLEV = 0.

Table A.1 NMOSFET noise simulation

Simulation Tools		HSPICE	PSPICE
Device model	SPICE level 3	Level 3 (noise model default: NLEV = 2)	Level 3 (noise model default: NLEV = 2)
	BSIM 3.2	Level 47 (noise model default: NLEV = 2)	Level 6 (noise model default: NLEV = 2)
	BSIM 3.3	Level 49 (noise model default: NLEV = 2. It does not recognize "noimod".)	Level 7 (noise model default: noimod = 1. It does not recognize "NLEV".)
Noise model	Noise model in SPICE level 3	NLEV = 0: $\overline{I_{nd}^2} = \frac{KF \bullet I_{ds}^{AF}}{C_{OX} \bullet L_{eff}^2 \bullet f}$ NLEV = 1: $\overline{I_{nd}^2} = \frac{KF \bullet I_{ds}^{AF}}{C_{OX} \bullet W_{eff} \bullet L_{eff} \bullet f}$ NLEV = 2 & 3 (default): $\overline{I_{nd}^2} = \frac{KF \bullet g_m^2}{C_{OX} \bullet W_{eff} \bullet L_{eff} \bullet f^{AF}}$	Same as left
	BSIM 3.2	Same as above	Same as above
	Noise model in BSIM 3.3	Same as above	noimod = 1 (default): $\overline{I_{nd}^2} = \frac{KF \bullet I_{ds}^{AF}}{C_{OX} \bullet L_{eff}^2 \bullet f^{ef}}$ (1) noimod = 2 (2):

Note: (1): According to our data, we believe that this expression should be NLEV=2 &3;

(2): The noimod = 2 noise model is as following from BSIM3.3 manual:

$$\overline{I_{nd}^2} = \frac{q^2 kT\mu_{eff} I_{ds}}{C_{OX} L_{eff}^2 f^{ef} \bullet 10^8}\{Noia \bullet \log\{\frac{N_0 + 2\times 10^{14}}{N_l + 2\times 10^{14}}\} + Noib \bullet (N_0 - N_l)$$

$$+ \frac{Noic}{2}\{N_0^2 - N_l^2)\} + \frac{V_{tm} I_{ds} \Delta L_{clm}}{W_{eff} L_{eff}^2 f^{ef} \bullet 10^8} \bullet \frac{Noia + Noib \bullet N_l + Noic \bullet N_l^2}{(N_l + 2\times 10^{14})^2}$$

3. HSPICE level 47 Simulation Program for flicker noise

This program is used to simulate the 0.6-um NMOS flicker noise by HSPICE level 47 (BSIM 3.2).

As in the previous PSPICE level 7 program, first, the transistor DC characteristics are matched to the experimental measured data by adjusting the parameters in the HSPICE models. After that, the noise characteristics can be simulated according to the noise experimental results using the appropriate noise equation selector (NLEV), flicker noise exponent (AF) and coefficient (KF) in HSPICE.

The output file of the HSPICE simulation also only gives the value of FN (output flicker noise at the drain node, V^2/Hz). We can calculate the drain current noise and the input-referred voltage noise in the same way as in the previous section.

```
NMOS Noise Simulation L=0.6um level 47 in HSPICE (BSIM 3.2)

VDD 3 0 dc=5V          % DC power supply at the drain node
VGS 1 0 dc=2V ac=1V    % DC, AC power supply at the gate node
Rg 1 2 1K              % resistive load at the gate node
Rd 3 4 100             % resistive load at the drain node
Cgs 2 0 100u           % additional gate-source capacitance

m1 4 2 0 0 ntran l=0.6u w=30.8u                % NMOS netlist
.MODEL ntran NMOS level=47 tox=95.0e-10 vto=0.7v kp=50e-06
                  % main parameters of DC characteristics
+ nlev=3 af=1 kf=1.0e-24     % noise model parameters
.ac dec 100 .01 2             % AC analysis
.NOISE V(4,0) VGS 10          % noise analysis
.dc VGS 1 4 0.5               % DC analysis
.probe             % write all analysis data to output file
.op                % calculate and print all dc node
                   % voltages and voltage source currents
.option post
.END               % end of PSPICE simulation input file
```

The HSPICE level 49 (BSIM 3.3) simulation program is almost the same as HSPICE level 47 (BSIM 3.2) except that the device model level selector changes to "level = 49". The PSPICE level 6 (BSIM 3.2) simulation program is about same as that of the PSPICE level 7 (BSIM 3.3), which is already shown above, except that the device model level selector changes to "level = 6".

As listed in Table A.1, the noise equations in HSPICE level 49, HSPICE level 47 and PSPICE level 6 are same where the same noise equation selector (NLEV) is specified in the simulation program. As stated in the HSPICE manual, the BSIM 3.3 noise model has not been installed [31]. The PSPICE level 7 uses a different noise equation selector, NOIMOD. This is why only PSPICE level 7 can simulate the input-referred voltage noise in the NMOSFET transistor as shown in Fig. A.4, which is same as Fig. 2.10 in Section II of this thesis.

Fig. A.3 shows the HSPICE level 49 (BSIM 3.3), HSPICE level 47 (BSIM 3.2) and PSPICE level 6 (BSIM 3.2) can closely simulate the measured drain current noise, but the PSPICE level 7 (BSIM 3.3) still gives the best simulation match.

Fig. A.4 shows that all the three simulation tools, HSPICE level 49 (BSIM 3.3), HSPICE level 47 (BSIM 3.2) and PSPICE level 6 (BSIM 3.2), predict that the input-referred voltage noise stays constant as the gate bias increases, which does not fit the measured input-referred voltage noise. The PSPICE level 7 correctly simulates that the input-referred voltage noise is proportional to the gate bias, increasing as the gate bias increases.

In other words, for NMOS transistor noise simulations, PSPICE level 7 (BSIM 3.3) is the most appropriate simulation tool.

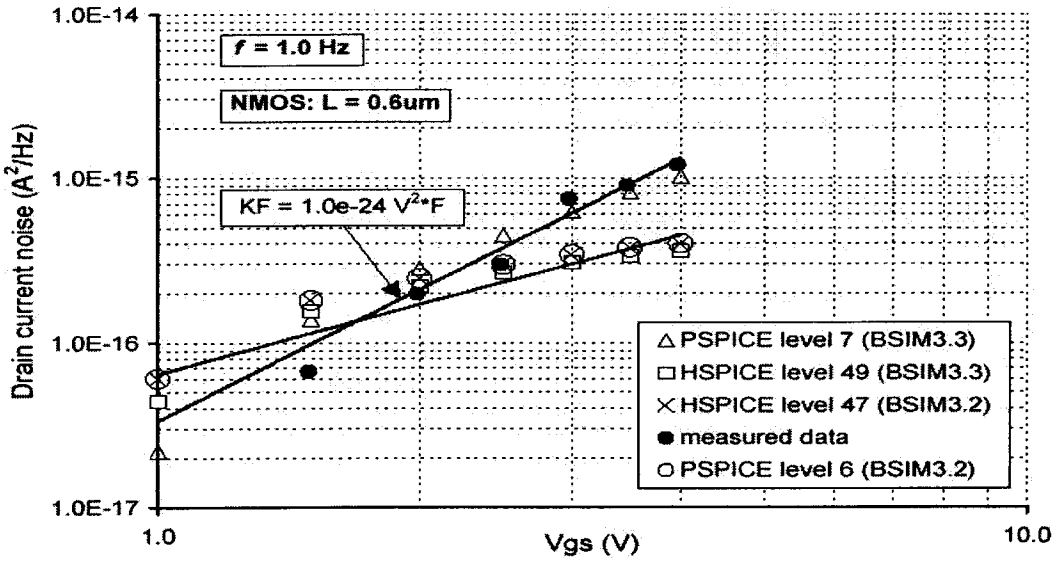

Figure A.3. Different SPICE models used to simulated the drain current noise for the 0.6-um short channel NMOS transistors in the saturation region. $f = 1$ Hz.

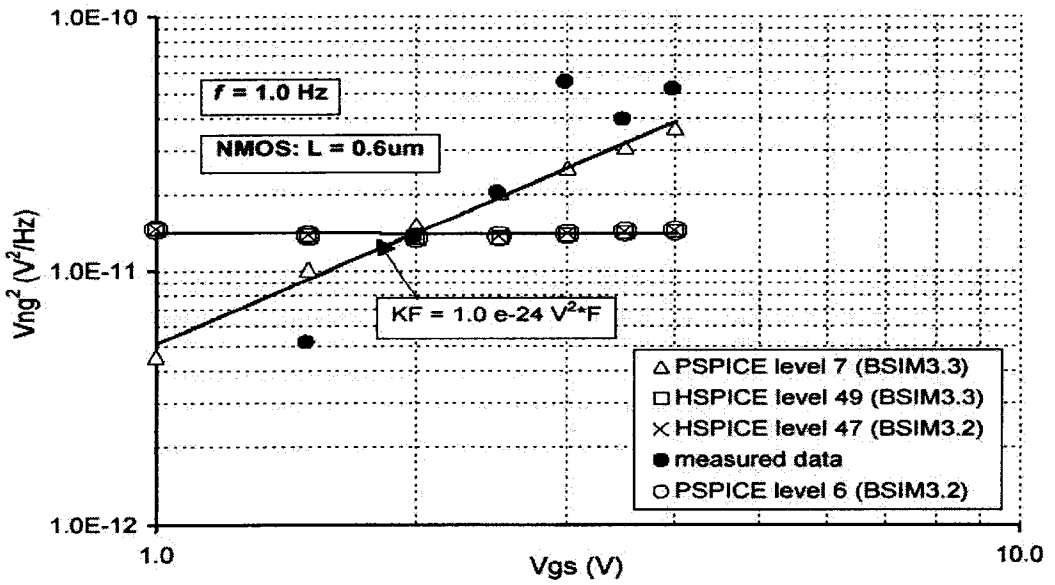

Figure A.4. Different SPICE models used to simulated the input-referred voltage noise for the o.6-um short channel NMOS transistors in the saturation region. $f = 1$ Hz.

4. MATLAB Program B

This program is for simulation of random-phase flicker noise in MATLAB. The details of the simulation are explained in Section III Part A of this thesis (pp. 22-26).

```
% NMOS Random-Phase Flicker Noise Simulation by Matlab

clear all; close all
W=120e-6; L=5e-6; Tox=1050e-10;    % NMOS physical dimension
epo=8.85*10^(-12);kox=3.9;uo=512; % known constants
AF=1; gm=0.3e-3;                   % known constants
Cox=epo*kox/Tox;                   % calculate Cox
KF=1.0e-13;                        % assumed KF value

% frequency changes from 10MHz to 1000MHz in steps of 10MHz
f=1e7:1e7:1e9;

% total MATLAB simulation time with 100ps sampling delay
t=0:1e-10:1e-7;

% HSPICE Level 2&3 1/f noise in NMOS
flicker=((KF*gm.^2)./(Cox*W*L*f.^AF));  % unit=A^2/Hz
Ind=flicker.^0.5;                       % unit=A/Hz^0.5

% amplitude of drain current noise
Iamp=Ind.*(1e7)^(1/2);                  % unit=A

rand('seed',sum(100*clock));      % rand function in MATLAB

% Save data into files for MS EXCEL use
     f1=f'; flicker1=flicker'; Iamp1=Iamp';
     outputdata1=[f1 flicker1]; outputdata2=[f1 Iamp1];
     save figure1.dat outputdata1 -ascii
     save figure2.dat outputdata2 -ascii

figure(1)
subplot(2,2,1)            % Figure 3.1 in the thesis
loglog(f,flicker,'-*'); grid on
%title('Modeling flicker noise with KF=5.9e-13)');
xlabel('Frequency  log  (Hz)');
ylabel('Flicker noise (A^2/Hz)'); zoom on
```

```
subplot(2,2,2)              % Figure 3.2 in the thesis
     loglog(f,Iamp,'*'); grid on
     title('Calculated amplitude of sine waves
            when KF = 1.0e-13 (V^2 F)');
     xlabel('Frequency  log  (Hz)');
     ylabel('Amplitude of sine waves (A)');
     zoom on

for i=1:length(f)
     x=rand(1);
     sum1(i,:)=Iamp(i)*sin(2*pi*f(i)*t(:)'+2*pi*x);
end
     sum2=sum(sum1);

subplot(2,2,3)                  % Figure 3.3 in the thesis
     plot(t,sum2); grid on
     xlabel('Time  (t)')
     ylabel('Sum of Sine waves with random phase (A)')
     title('Sum of sine waves with random phase
            when KF = 1.0e-13 (V^2 F)');

% Save data into file for HSPICE simulation and EXCEL use
     t1=t'; sum3=sum2';
     outputdata3=[t1 sum3];
     save figure3.dat outputdata3 -ascii

% 1/f noise with random phase
% data is taken from Matlab simulation
load 'figure3.dat'        %CMOS 100000 data
time=figure3(:,1);
noise=figure3(:,2);
fs=1e10;                  % sampling frequency
L1 = length(noise); % L is also a window size. As L get
                    % larger magnitude of fft gets closer
                    % to theoritical value
L=1024;
%SETUP AXIS
f1 = fs.* ( 0:1/L1:1-1/L1 ); % up to f=fs
a = L/2;
a = round(a);
f = f1(1:a);              % up to fs/2

mag = fft(noise,L); % L is the size of windows

% Power Spectral Density (PSD)
power = mag.* conj(mag) /(1e10 * L);
power = power(1:a);
```

```
subplot(2,2,4);                    % Figure 3.4 in the thesis
     loglog(f,power,'*')
     axis([1e7,1e9,1e-18, 1e-14]); grid on;
     title('Power spectral density of the sum of sine waves
            with random phase. The original KF value is KF
            = 1.0e-13 (V^2 F)');
     xlabel('frequency  log  (Hz)');
     ylabel('PSD of the Sum  (A^2/Hz)');
     hold on,
     loglog(f,1e3./f.^1,'k'), text(2e8, 1e-5, '1/f');
     zoom on

% Save data into file for EXCEL use
     f2=f'; mag1=power;
     outputdata4=[f2 mag1];
     save figure4.dat outputdata4 -ascii

HOLD OFF
```

5. HSPICE Simulation Program for Phase Noise

This program is for HSPICE simulation of phase noise effects on the 2-GHz CMOS LC oscillator. The detail information for the simulation is explained in Section III Part B (pp. 26-31).

```
*LC CMOS oscillator simulation in HSPICE (with 1/f noise)

Vdd 1 0
+ pulse(0 3 0.00001u 0.00001u 0.00001u 5u 5.00000001u)

L1 3 4 3.2e-9                    % Inductance, unit=H
L2 3 5 3.2e-9

R1 4 6 6.35                      % Resistance, unit=Ohms
R2 5 7 6.35

C1 6 0 1.22e-12  IC=0            % Capacitance, unit=F
C2 7 0 1.22e-12  IC=3

M1 6 7 0 0 N W=400u L=0.7u
+NRS=0.0025 NRD=0.0025 AD=800p PD=800p AS=800p PS=800p

M2 7 6 0 0 N W=400u L=0.7u
+NRS=0.0025 NRD=0.0025 AD=800p PD=800p AS=800p PS=800p

M3 3 2 1 1 P W=800u L=0.7u NRS=0.00125
+NRD=0.00125 AD=1600p PD=1600p AS=1600p PS=1600p

M4 2 2 1 1 P W=800u L=0.7u NRS=0.00125
+NRD=0.00125 AD=1600p PD=1600p AS=1600p PS=1600p

RBIAS 2  0  2000

.model P pmos level=3 ld=0.0u wd=0.4u vto=-0.9 tox=200e-10
+uo=180 nsub=2.8e16 vmax=1.9e5 eta=0.09 theta=0.13
+kappa=0.3  delta=0.3  xj=0.0  nfs=1e12  rsh=1400  rd=0  rs=0
+rg=0   rb=0   cgdo=1.85e-10   cgso=1.85e-10   cgbo=2.5e-10
+cj=5.2e-4  cjsw=2.8e-10  mj=0.5  mjsw=0.33  js=1e-3  fc=0
+pb=0.9
```

```
.model N nmos level=3 ld=0.15u wd=0.3u vto=0.73 tox=200e-10
+uo=520   nsub=2.8e16   vmax=1.35e5   eta=0.02   theta=0.07
+kappa=0.1  delta=0.6  xj=0.1u  nfs=5e11  rsh=650  rd=0  rs=0
+rg=0   rb=0   cgdo=1.85e-10   cgso=1.85e-10   cgbo=2.5e-10
+cj=3.2e-4  cjsw=2.8e-10  mj=0.95  mjsw=0.12  js=1e-3  fc=0
+pb=0.8

.include flicka.dat % this data file comes from last MATLAB

.options ACCURATE=1
.option post
.op
.tran 0.00489e-10 0.0489u    % this value is very important
*.print tran V(7)

.fft v(7) np=2048  window=harris   % fast Fourier transform

.END
```